



Stiction Free Fabrication of MEMS Devices with Shallow Cavities Using a Two-Wafer Anodic Bonding Process

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Abstract

MEMS devices often employ free standing structures, such as beams and plates, over a cavity that allows space for structures to bend or oscillate, and also acts as a dielectric medium for the electrostatic field between the structure and the electrode placed at the bottom of the cavity. Such cavities are common in inertial and acoustic sensors. In order to create these cavities, a sacrificial etch is used in traditional fabrication methods such as surface micromachining. The sacrificial etch and release is a tricky process that often leaves structures only partially released. In addition, if the free structure is a large plate or membrane as in the case of MEMS gyroscopes, the sacrificial release requires many etch holes that may not be desirable in the structure. Here, we describe a two-wafer process in which the sacrificial release step for creating cavities, and hence the problem of stiction, can be avoided altogether. This process involves anodic bonding of the two wafers that is easily optimized for the desired result. We discuss the process first on a test structure and then show how we successfully use this process to fabricate a two-mass vibratory gyroscope.

1. Introduction

There have been two dominant fabrication methods for silicon micromachining, broadly classified as bulk micromachining (etching deep features into a wafer) and surface micromachining (depositing, patterning, and selective etching of films on a wafer). Fundamentally, both of these techniques rely on some form of etching or material removal. A complementary, additive, micromachining technology is the wafer-to-wafer bonding of patterned substrates, often simultaneously involving alignment of the substrates.

While fabricating large area structures such as microphones and CMUTs using surface

micromachining, the sacrificial release invariably leads to the stiction phenomenon. Even if dry etching is used, the residual stress in the structure leads to the warping of the structure during release (refer to fig.1a and 1b). The issue is more severe when realizing gaps of the order of a few hundred nanometers. The realization of a closed cavity is difficult using a surface micromachining technique. Typically closed cavities are created by etching the sacrificial layer below the structure through etch holes in the structure. The etch holes need to be sealed after release of the moving structure in some applications. This process is tedious and often leads to only partially released structures.

Wafer bonding is a preferred alternative when

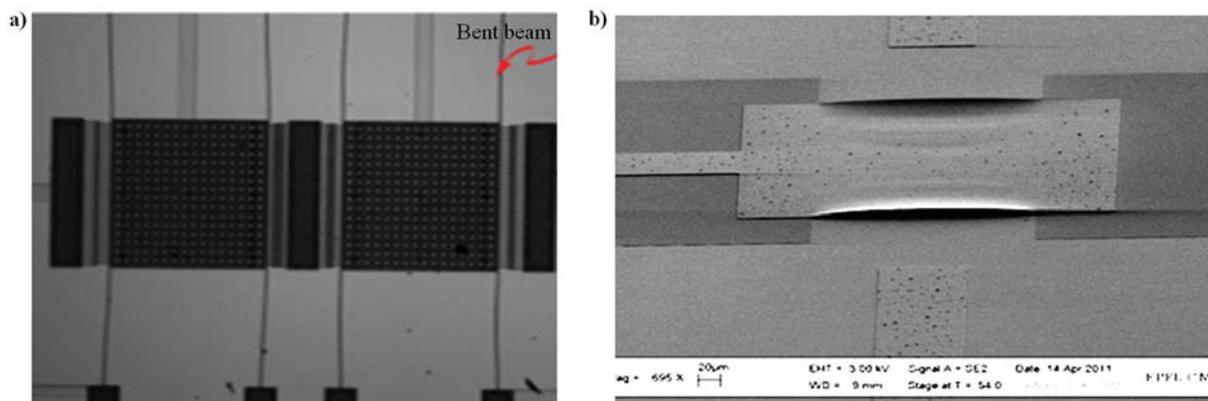


Figure 1. (a) A surface micromachined gyroscope [Mohite *et al*, 2006] showing severely bent beams due to the residual stress induced during realization (b) The curling of plate edges in a FET based microphone during sacrificial release*. *Courtesy Charanjeet Kaur.

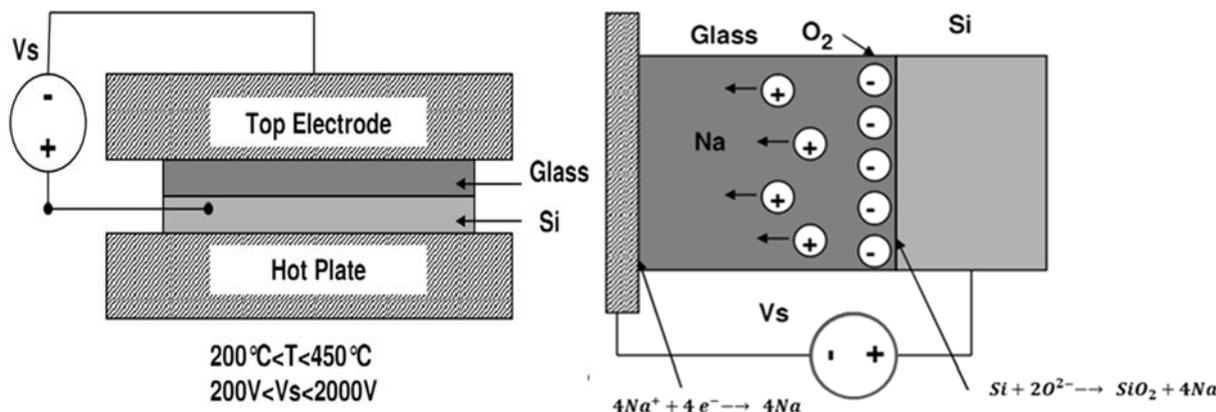


Figure 2. (a) Schematic diagram of anodic bonding setup (b) Anodic bonding mechanism [Warren]

realizing gaps of less than a micron below large area structures such as a membrane of $500 \times 500 \mu\text{m}^2$ or higher. It is also possible to get sealed cavities using this technique. This wafer bonding technology is most efficient in realizing 3D MEMS devices. This technology is advantageous in the fabrication of multi layered devices and has been successfully used up to 7 wafer stack bonding in realizing a micro turbine by M.Schmidt at MIT [Londona *et al*, 2001].

In this paper, we present the results obtained by anodic bonding and its application in realizing structures with a cavity. The cavity thus fabricated is characterized using a Scanning Acoustic Microscope (SAM). We further demonstrate how this technique can be applied for realizing a silicon micromachined gyroscope.

2. Anodic bonding and comparisons with other wafer bonding methods

The field assisted bond was initially developed for the bonding of metals to glass, and subsequently the metal was replaced by silicon [George, 1975]. Details of this process are available in the standard literature such as reference [Londona *et al*, 2001]. However, for the sake of the discussion that follows, we include here a very brief description.

The silicon-to-glass anodic bonding process is shown schematically in fig. 2. The glass wafer is in contact with a cathode, and the silicon wafer acts as an anode. The contacted wafers are heated to $300\text{--}400^{\circ}\text{C}$ while a voltage between $200\text{--}800\text{ V}$ is applied in steps. Under such a high field

Table 1. A comparative study on various wafer bonding techniques [Warren]

	<i>Anodic</i>	<i>Fusion</i>	<i>Glass frit</i>	<i>Eutectic</i>	<i>Solder</i>
Bond strength	Very strong	Excellent	Strong	Strong	Strong
Hermeticity	Good	Excellent	Good	Good	Good
Temperature	250-400 °C	200-1000°C	400-500°C	>363°C	57-400°C
TCE mismatch	Ok	Good	Ok	Ok	Poor
CMOS compatible	Ok	Poor	Ok	Ok	Good
Process complexity	Low	Some	Some	Some	Some
Maturity	Decades	Many years	Many years	Many years	Years

and elevated temperature, the mobile Na^+ cations in the sodium rich glass migrate away from the bonding interface, leaving behind negatively charged oxygen ions in the glass that create a high electric field across the bonding interface with image charges in the silicon. At these temperatures and high electric fields, a chemical bond between the silicon and oxygen forms, resulting in the Si-SiO_2 – glass bond that holds the wafers together. The primary variables that control this process are temperature, time, and voltage. It is important to pay attention to the thermal coefficient matching between the two materials at the process temperature. The oxygen bonds to the Si atoms at the surface, creating a very strong SiO_2 bond. The two wafers are permanently bonded together since the SiO_2 bond is actually stronger than the Si-Si bond or the Pyrex glass.

Table 1 shows a comparison of anodic bonding with other bonding methods. It can be seen that anodic bonding offers a low temperature process and a relatively simple method of fabrication when compared to all the other methods of wafer bonding.

3. Experimental method

3.1 Cavity formation with Plaza Test Pattern and Glass to Silicon Anodic Bonding

We take a glass wafer with pre-processed dimples and a silicon wafer (see fig. 3), bond them together using the anodic bonding process described in section-2 to form a cavity shown in fig. 3(c), and conduct experiments to test the bonding and uniformity of the cavity.



Figure 3. (a) Pre-processed glass wafer (b) Silicon wafer (c) Bonded wafer

We adopt the test protocol proposed by Plaza *et al* [1997] to measure the bond quality by comparing the electrostatic pressure to bond strength. We make a Plaza test mask, shown in fig. 4(a), to create surface cavities on the glass wafer as shown in fig. 4(b). We subsequently bond the

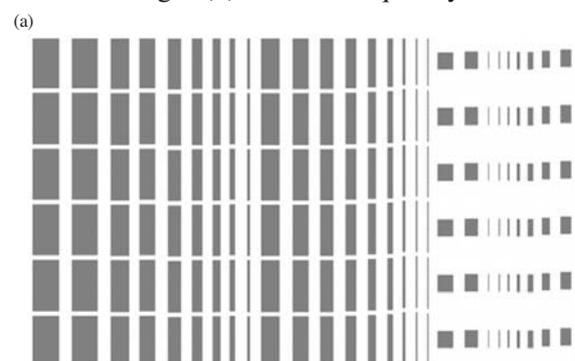
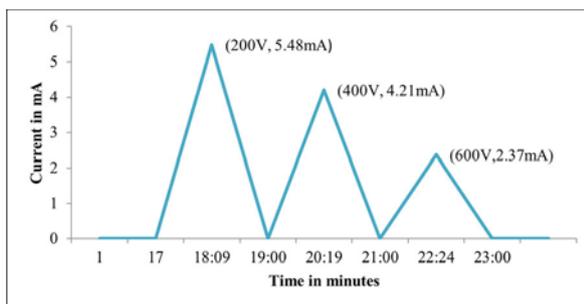


Figure 4. (a) Mask plate having the Plaza test pattern (b) Plaza test pattern etched 7740 glass substrate

Table. 2 Process parameters for the Plaza mask test

Process parameters: EVG 501 series	
Chamber pressure: 5x10 ⁻² mbar	Pyrex glass thickness: 450 μm
Chamber temperature: 400 °C	Etchdepth using RIE: H ⁺ 1.2 μm
Voltages increment steps: 200 V, 400 V, 600 V	Gap between etch patteren: 500 μm
Silicon thickness: 250 μm-P type	Minimum feature size: 20 μm

**Figure 5. Current-time characteristics during the bonding process with recorded values marked at each current peak on the curve.**

two wafers. The process parameter values are recorded on the bonder to check the bonding condition. The details are presented in table 2 and fig. 5.

Fig. 5 shows the current peaks that are generated during various applied voltages. Decreasing peaks are indicative of increasing SiO₂ thickness in the bonded zone. This leads to a low magnitude current peak at the corresponding applied voltage. The current curve is the primary indication of bond formation between the two wafers.

The influence of the bonding conditions on the bond quality was measured by calculating the electrostatic pressure [Plaza *et al.*, 2005] needed to form a bond between the two surfaces with a fixed separation. If the structure remains bonded, then the bond force is assumed to be larger than the elastic restoring force equivalent to the electrostatic pressure. The bonding of the structures is a function of the mask variables (width and etch depth), process variables (voltage and temperature), and ion mobility, etc. The bond quality was characterized in two steps: first, with a visual inspection to

see which Plaza test structures actually bonded, and then with a calculation of the electrostatic pressure determined by the applied voltage and etch depth given by

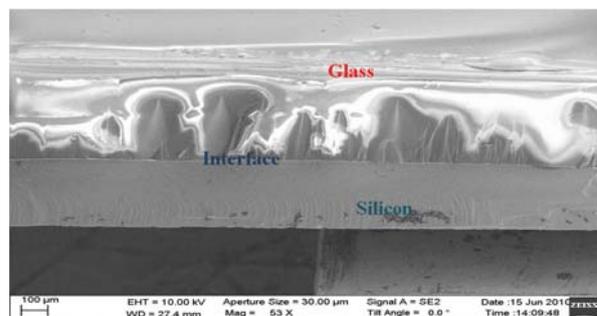
$$P = \frac{1}{2} \epsilon_0 \left(\frac{V^2}{H^2} \right)$$

Where P is the electrostatic pressure, V is voltage, H is depth of the cavity and ϵ_0 is relative permittivity.

From this experiment for Plaza tests we concluded the following:

- The bond was uniform and no bending was observed.
- The bond strength was found to be higher than the Si-Si bond (during a strength test the Pyrex glass broke before the crack propagation at the bond interface).
- The interface bond and glass had a similar composition since nothing was reflected from the interface in an FTIR (transmission) analysis; the spectrum was completely absorbed by the SiO₂ content in the Pyrex glass. .

We also did a cross-sectional SEM (Scanning Electron Microscopy) imaging (see fig. 6) to check the interface between the two wafers. The materials bonded, silicon and pyrex glass, have similar coefficients of thermal expansion within the bonding temperature range of 275-350 °C [Debura, 2004]. Hence only negligible residual stress is expected at the junction. The reliability of the bond needs to be studied separately using accelerated testing techniques.

**Figure 6. Scanning Electron Microscopy image of anodically bonded interface.**

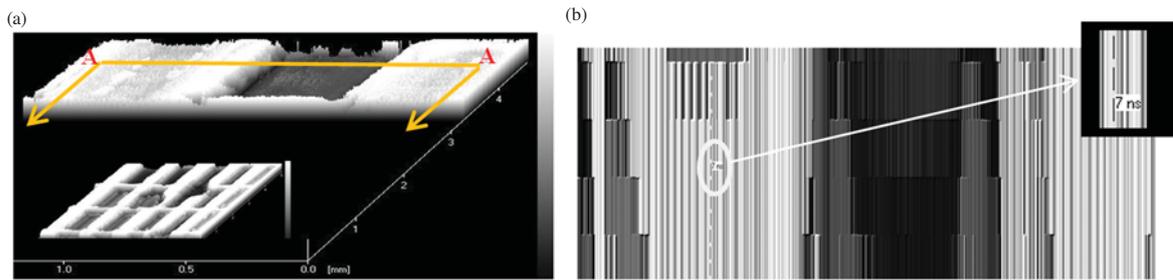


Figure 7. (a) Surface topology at the bonded interface as seen by Scanning acoustic microscopy (b) The cross sectional view of the sample and time of flight for the acoustic signal to reach the bottom of the cavity. The time of flight, 7 nsec, is shown in the zoomed view as displayed by the SAM.

3.2 Characterization: Cavity thickness Measurement

SAM (Scanning Acoustic Microscopy) is a nondestructive imaging technique that can be used for determining the uniformity of the bonded wafer pairs at the interface [Tan *et al.*, 2011]. C-mode scanning is employed to examine the interface of the bonded wafer pair. C-mode provides a display of the image of relected echoes at the focused plane of interest, or acoustical data collected along an X–Y plane at depth Z, thus furnishing a two-dimensional (area) description at a particular depth (Z). Fig. 7(a) shows a 3D image of the bonded wafer indicating the bond interface and the air cavity depth. The sealed cavities are represented by the ‘dark squares’ of various sizes that are uniformly distributed across the entire wafer. TA numbers of weakly bonded patches (identified by the lighter contrast) are also seen at the center of the sample.

The thickness of the air cavity is easily

determined using the time of flight recorded by SAM as follows.

Thickness of the cavity = $0.5 \times$ time of propagation of acoustic wave in cavity \times sound speed in the air medium.

$$= 0.5 \times 7 \times 10^{-9} \text{ sec} \times 330 \text{ m/sec} = 1155 \text{ nm} = 1.155 \mu\text{m}.$$

Thus we achieved our goal of creating a shallow cavity of $1.1 \mu\text{m}$ without involving any sacrificial release and thus avoiding the problem of stiction. We now describe an example fabrication for a gyroscope structure using the bonding process detailed above.

4. Gyroscope Fabrication

Geometry: The gyroscope structure [Nishad, 2006] of interest consists of two large proof masses (size $500 \times 500 \mu\text{m}^2$) suspended with $500 \mu\text{m}$ long beams over a cavity of depth $1 \mu\text{m}$ (see fig. 8).

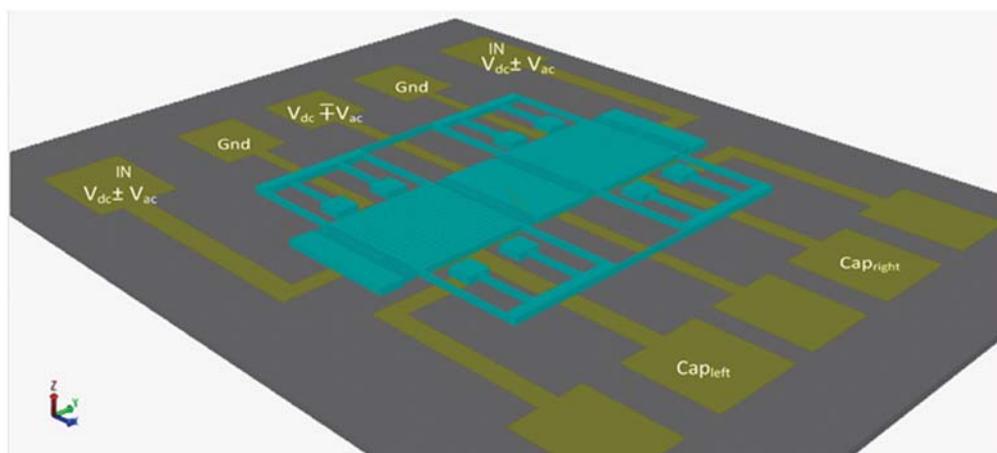


Figure 8. Schematic gyroscope structure [JP Reddy, 2010].

The process flow for fabricating this structure using a two wafer process [William, 2005] is shown in fig. 9.

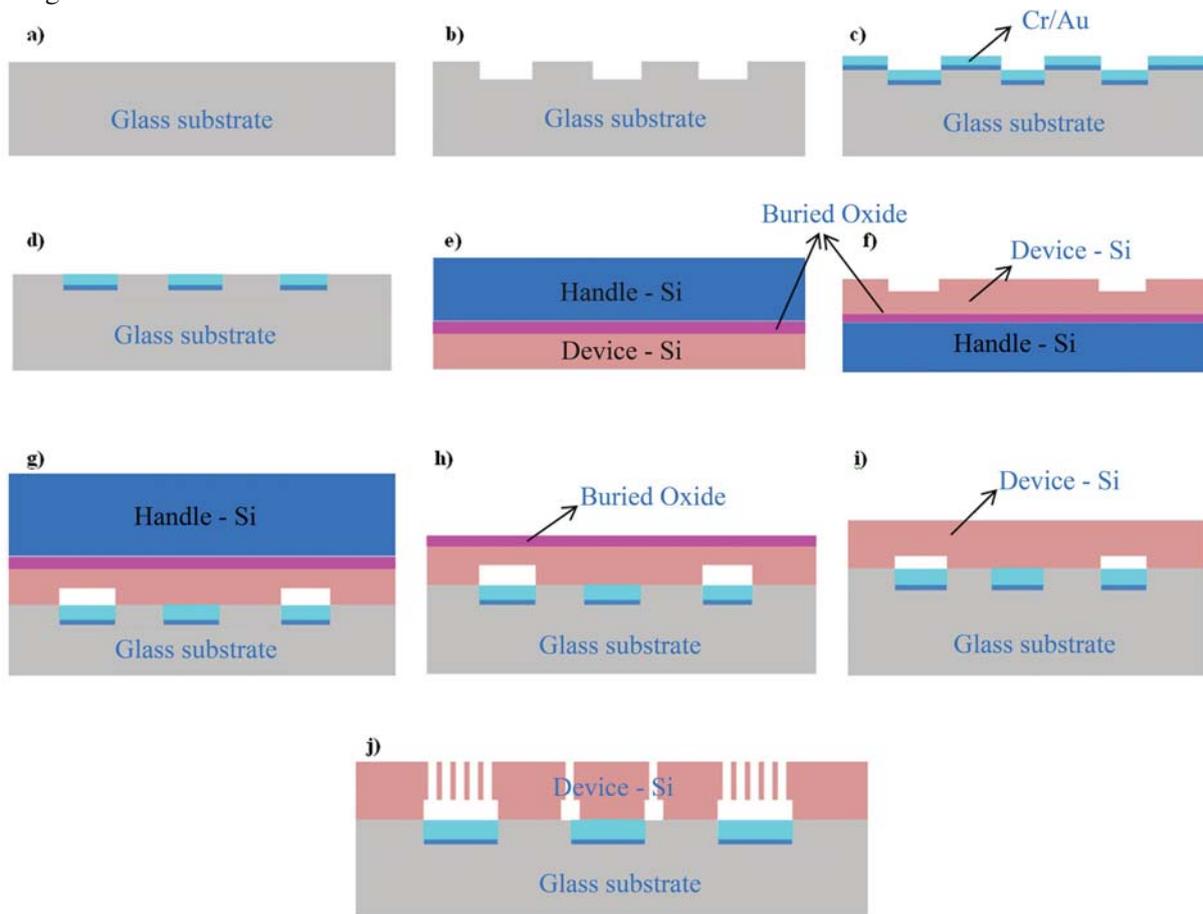


Figure 9. Fabrication process flow for Gyroscope (a) Pyrex glass (b) Patterning electrode mask (c) Deposition of electrode (d) Lift off (e) SOI wafer (f) Patterning dimple mask (g) Aligned anodic bonding (h) Blanket etching of handle layer of SOI (i) Blanket etching of oxide layer (j) Patterning and etching of structural mask

The process involves three lithography steps and is inclusive of the contacts needed for probing connections.

In the bonding process, the major issue is to ensure that the structure does not bend during bonding. For verifying the allowable areas and the vertical gaps that can be successfully bonded without warping, we carried out the Plaza test on dummy structures. The details of the areas considered during the Plaza test are given in table 2. The maximum and the minimum areas considered were $1100 \mu\text{m} \times 1500 \mu\text{m}$ and $20 \mu\text{m} \times 500 \mu\text{m}$ respectively. The air gaps targeted were about $1.2 \mu\text{m}$ deep and were etched as cavities in the glass wafer. Fig. 4 shows the bonded sample carrying dummy patterns.

Fig. 10 shows the major steps involved in the

anodic bonding process in realizing the gyroscope. The process parameters recorded during the bonding process are listed in table 3, and fig.11 shows the time-current recordings during the process. From fig. 11 we notice that the magnitudes of the current peaks are higher compared to those in the Plaza test (fig. 5). This is because of the presence of the gold metal interface layer between the glass and the silicon. This metal layer, used for electrodes in fabrication, introduces another interface layer in the bonding process leading to the triple bond discussed below.

4.1 Triple bonding

The metal layer present between the glass and silicon is not a continuous layer since it is already patterned in the form of electrodes. Therefore, at the bonding interface, we do not have a continuous

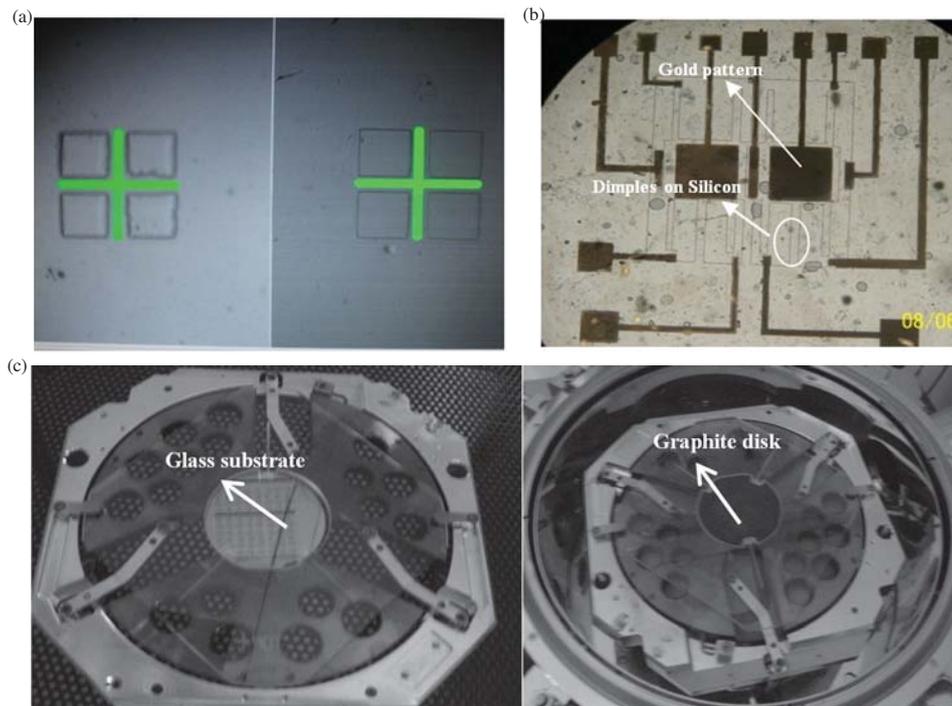


Figure 10. (a) Easy back side alignment is due to transparency of the glass (b) Device level alignment (c) Anodic bond setup with graphite electrode on top

Table 3. The process parameters for anodic bonding of the gyroscope wafers

Process parameters: EVG 501 series	
Chamber pressure: 5×10^{-2} mbar	Pyrex glass thickness: 450 μm
Chamber temperature: 398 $^{\circ}\text{C}$	Etchdepth using RIE: H^+ 1.2 μm
Voltage increment steps: 200 V, 400 V, 600 V	Gap between etch patternen: 500 μm
Silicon thickness: 350 μm -P type	Minimum feature size: 20 μm

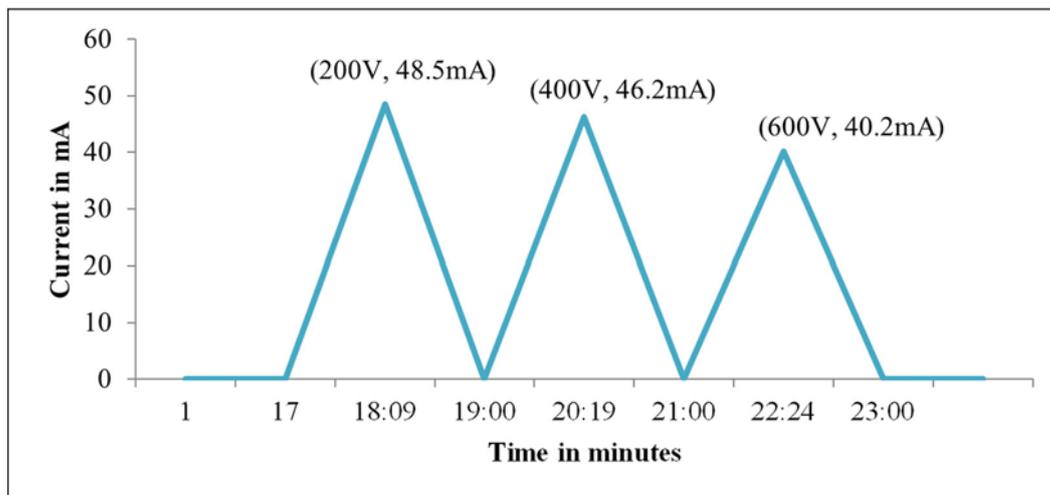


Figure 11. Current characteristics of the anodic bonding process for the metal coated wafer.

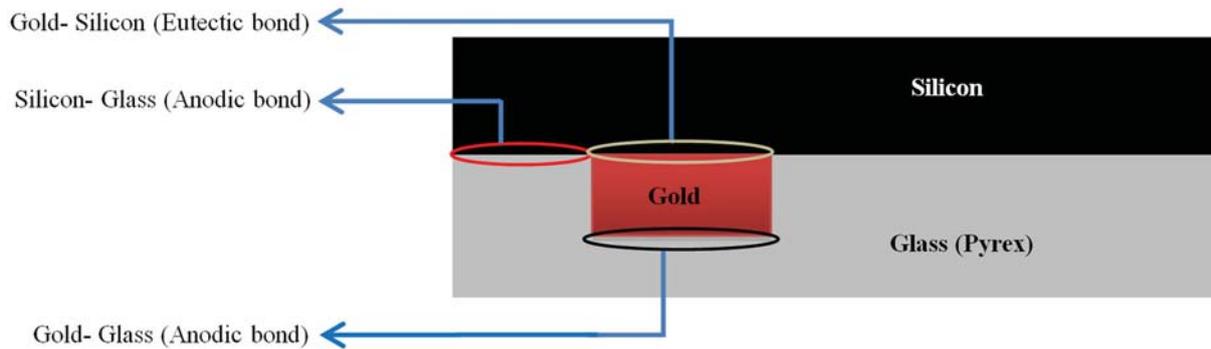


Figure 12. Triple bond configuration in realizing a Gyroscope

single material boundary on the glass side. This situation is schematically shown in fig. 12. As a consequence, there are three interfaces that participate in bonding. These three interfaces bond differently using appropriate bond chemistry: Glass-Silicon anodic bond, Silicon-Gold Eutectic bond and Gold-Glass anodic bond.

4.2 Realized structure

Fig. 13 shows one of the steps in realizing the MEMS gyroscope by anodic wafer bonding method and it refers to the fig. 9(i) step in the process flow.

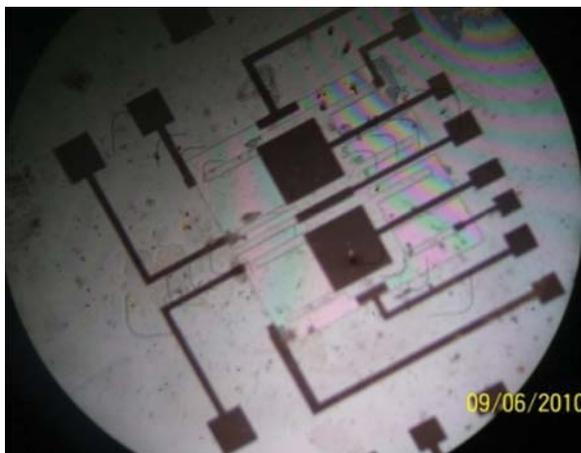


Figure 13. Realization of the bonded device with proper alignment

5. Conclusions

We have demonstrated a simple method using silicon and glass wafer bonding for realizing a MEMS gyroscope. The glass substrate material used is Pyrex #7740 which is relatively inexpensive. It can also be used for realizing closed cavities

needed in CMUTs and microphones. In addition, since the glass is transparent, the back side alignment of the mask layer is easier with the method presented. In the case of the Si-Si bond, the limitation is the infrared camera rear alignment process. Though it was not verified, but the residual stresses in the structural member would be negligible when compared to that obtained by other fabrication methods. At the bond interface, the formation of SiO_2 during bonding is likely to help in avoiding the leakage current for the electronics. The anodic bond used in this work is also suitable for hermetic sealed device packaging.

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