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Fringe Field Junctionless FET as a Sensitive Displacement Sensor

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Zepto farad

Abstract

This paper reports a novel transduction proposition with merits of good sensitivity using a Junctionless FET to pick-up inertial changes in MEMS or NEMS devices. Here the NEMs gate is displaced in an out-of-plane direction when subjected to any external vibrations. The displacement is assumed to be a forced plate motion. The resulting change in the gate fringe field due to this displacement modulates the drain current of the Junctionless Field Effect Transistor (JLFET). The displacement induced fringe field change (relative to the FET channel and the Ground planes) brings out a distinct shift in the I_{DS}-V_{GS} characteristics of the JLFET. When the gate displacement is in a few nano-meters (less than 5nm) range, the fringe field effect is dominant and the gate voltage required to deplete the channel to force an eventual turn-off tends to decrease. For 2nm displacement, the JLFET with a channel doping of $N_D = 8X10^{18}$ cm^{-3} operating at a bias point of V_{GS} = - 47.7V, we observe 2-orders of magnitude change in I_{DS} (nearly 98% change). We show that the equivalent change in capacitance measured in this technique is in a few zepto farads. TCAD 3D simulations are presented to validate the sensitivity of the Fringe Field JLFET (FF-JLFET).

1. Introduction

Tracking nanometer range displacements in MEMs or NEMs devices is a challenging task considering the finer capacitance change arising out of these minuscule displacements. The prominent transduction principles can be classified into three categories as follows:

- Transduction principle based on changes in capacitance values
- Transduction principle based on the frequency shift observed in resonant devices
- FET integrated built-in transduction.

In the transduction principle based on capacitance change [Geen et al., 2002][Lotters et al., 1999; Hegde, 2009], the signal conditioning platform should be highly immune to the effect of parasitics. This principle has limitations going beyond attofarad levels. In the resonant transduction principle, the signal conditioning complexity is quite prominent [Abele et al., 2005] and in the case of FET integrated built-in transduction [Wilbertz et al.,] the sensitivity offered is not high enough for many applications. Recently in [Song and Ajmera et al., 2009], the movable MEMS beam was coupled as a gate to the FET biased in saturation. Here, any change in the gate displacement due to external vibrations results in the variation of the gate overlap of the FET along the width direction. This, in turn, brings about a linear change in the drain current. The minimum detectable displacement in this approach is 1μm and the reported sensitivity is

5.8μA/μm which translates to a 1.4% change (if expressed as ($\Delta I_D / I_D$) x 100). This approach is not suitable for sensing displacements in the nanometer range. Fringe field modulation is used as a sensing principle in a MEMS motion sensor [Langfelder et al., 2011]. Here, the fringe field coupling is modulated by the displaced gate acting as a field sink. The reported sensitivity in this case is 50aF/25nm which translates to a 5% change in capacitance (if expressed as (ΔC/C) x 100). Extending this approach to smaller displacements of less than 10nm is challenging due to the dominant parasitic effects. In this context, JLFET has attracted considerable attention.

2. Junctionless FET as VB-FET

A Junctionless FET (JLFET) [Colinge et al., 2010] has created interest in the CMOS domain due to its near ideal sub-threshold slope of 60 mV/dec, reduced short channel effects and relative ease of fabrication compared to the bulk FET. This has been used as a NEMs RF resonator [Abele et al., 2005] opening up avenues for the possible exploration of this device in the NEMS domain. The JLFET is excited at a specific resonant frequency laterally and is shown to exhibit superior transmission characteristics at MHz operating frequencies [Grogg et al., 2011]. The channel is used as the Vibrating Body as shown in figure 1 and the gates are fixed and symmetric.

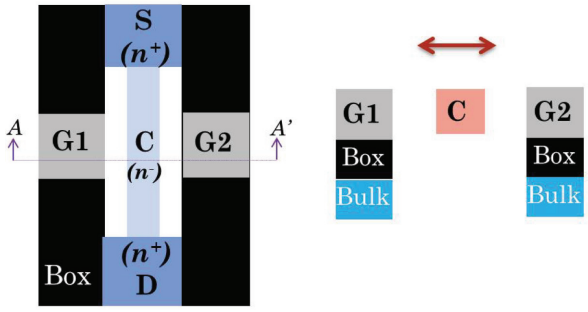


Fig. 1 (a) State of the art lateral VB-FET Top View. The gates G1 and G2 are fixed and the suspended channel portion (C) is laterally excited. (b) Crossectional view along A-A'[Grogg et al., 2011]

As the VB-FET in principle operates by turning the channel 'off' and 'on' at high frequencies, this approach cannot be used for inertial sensing to track minuscule displacements. Typically, the Source-Channel-Drain (S-C-D) in the JLFET are doped as n^+-n^--n^+. The JLFET is 'On' considering n-type dopant atoms and a -Ve gate bias needs to be applied to deplete the channel and turn-off the JLFET. This voltage is referred to as the pinch-off voltage (V_p).

3. Proposed Device Architecture

Our primary focus is on sensing very small nanometer displacements, typically less than 5nm using a Fringe Field JunctionLess Field Effect Transistor FF-JLFET. The proposed FF-JLFET could be classified under the third category of built-in transduction listed above and is constructed on a SOI substrate. It comprises a highly doped n+ source/drain $N_D = 1X10^{20}cm^{-3}$ to reduce the contact resistance and an n^- channel with a doping of $8X10^{18}cm^{-3}$ to result in the n^+-n^- -n^+ configuration of the S-C-D as in the Junctionless FET theory [Colinge et al., 2010]. The gate of the JLFET is a MEMs / NEMs comb finger which is attached to the proof mass as shown in figures 2 & 3. The proof mass motion in the Z-direction is assumed to be a 'forced plate motion' for small nanometer displacements. The comb finger hence also exhibits a forced plate motion in the Z-direction. The MEMS device comprising the proof mass and the comb finger is formed using a stack of a buried oxide (BOX) layer and an SOI Si film as seen in the cross section image figure 4. The BOX layer serves as the added mass layer for better mechanical sensitivity. It may be noted that the BOX layers in standard SOI substrates are available with various thicknesses ranging from 50nm to 1μm. NEMs / MEMs devices could be designed with a suitable choice of BOX and then coupled with the FF-JLFET. The Ground Planes (GP1 & GP2) are spaced at an equal distance with respect to the gate and the channel of the JLFET. The tip of the comb finger is coupled to the JLFET through a 50nm air gap. The comb finger now acts as the gate of the JLFET. Figure 2 shows the top view of the proposed FF-JLFET with gate coupling on either side. Figure 3 shows the isometric view of the FF-JLFET device in the Synopsys TCAD simulation environment. Taking symmetry into account in the rest of the paper for simulation / discussion purposes we use one comb finger interfaced onto a JLFET as in Fig. 3.

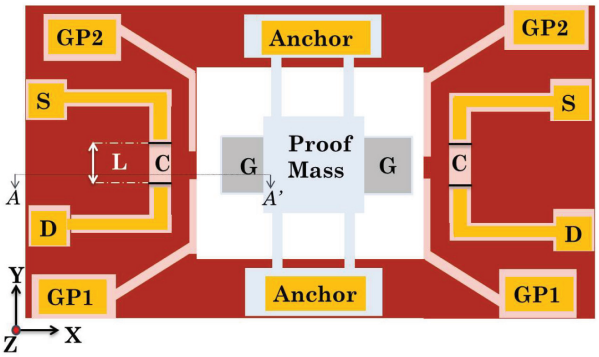


Fig. 2 Top View of FF-JLFET showing the movable gate (G), ground planes GP1, GP2 and the JLFET Source (S), Drain(D) and channel (C)

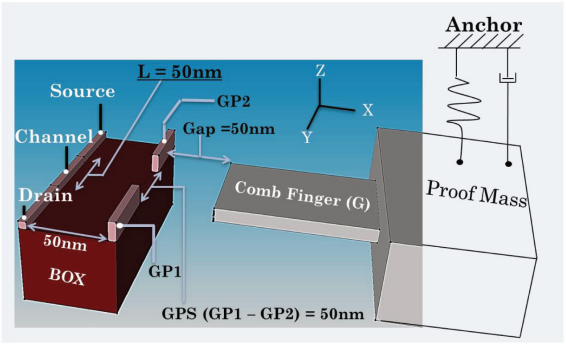


Fig. 3 FF-JLFET Isometric View used for simulation purposes: Here the comb finger acts as the JLFET Gate. Thickness of the comb finger acting as JLFET Gate = 5nm (along +ve Z-axis), Length of the JLFET Gate = 70nm (along Y-axis), GP1&2= Ground Planes. JLFET channel length (L) = 50nm, JLFET channel width (W) = 5nm (along -ve X-axis), JLFET channel thickness (t) = 5nm (along +ve Z- axis, Box thickness = 50nm. GP1& 2 width = 5nm (along +ve X-axis). Thickness of GP1&2 =13nm (along +ve Z-axis). S/D doping= $1X10^{20}cm^{-3}$, Spacing between the two Ground planes (GP1 - GP2) = GPS = 50nm; Gate overlap with GP1 = 10nm; Gate overlap with GP2 =10nm.

The channel width (W) and doping concentration (N_D) of the channel in a JLFET decide the pinch-off voltage. The width (W) of the JLFET is chosen to be 5nm to achieve a relatively lower pinch off voltage. The doping concentration, however, has a major impact on the sensitivity of the FF-JLFET and hence is chosen to be higher ($8X10^{18}cm^{-3}$). Figure 4 and Figure 5 show the cross-sectional view of the FF-JLFET along A-A'. The Ground Planes are not visible in this line of cross-section.

4. Operational Principle of FF-JLFET

The principle of the FF-JLFET is as follows. Initially, the NEMs gate is aligned with the JLFET channel ($\Delta Z = 0$) as in figure 4. Assuming forced plate motion when the proof mass (and, hence, the gate) experiences a displacement of 2nm, it is seen that the overlap area between the NEMs gate and the JLFET channel is partial as in figure 5.

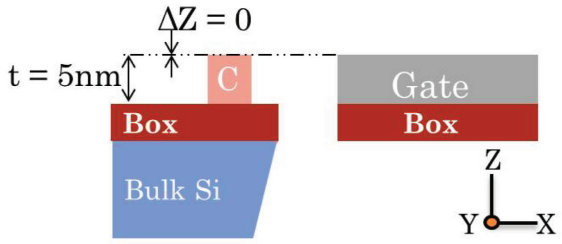


Fig. 4 Crossectional view of FF-JLFET along A-A'. When gate displacement ΔZ = 0. C is the channel which is stationary

For a small change in the gate (comb finger) displacement the field coupling between the gate and the channel changes because of the fringe field modulation. This effect is not prominent in the absence of the ground planes (GP1 & GP2). This is because the fringe field spreads at all possible angles before getting terminated onto the JLFET source which is grounded. As a result of this, the I_{DS}-V_{GS} curves, with and without gate displacements would overlap. However, upon the introduction of GP1 & GP2, the fringe fields are subjected to a level of screening. The GP1&2 (biased at zero potential) are introduced to act like a field sink to help terminate the fringe field lines outside the gate-channel-overlap-zone.

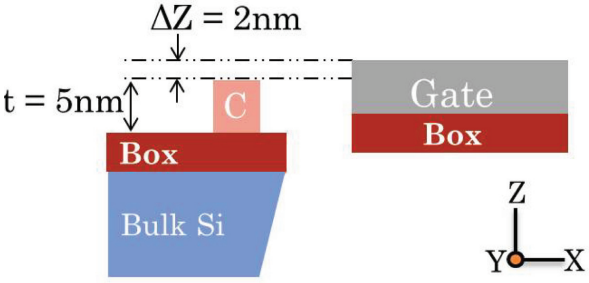


Fig. 5 Crossectional view of FF-JLFET along A-A'. Exaggerated view when the gate displacement ΔZ = 2nm along +ve z-axis.

Ignoring the fringe coupling through the BOX layer which is less significant, it is seen from figure 6 that the field coupling when $\Delta Z = 0$ is lower than the field coupling when $\Delta Z = 2$nm. This is due to the extra fringe field being coupled from the

displaced gate area terminating onto the top face of the JLFET channel; which more than compensates for the reduced physical overlap area as shown in figure 6. Besides the fringe field shown in figure 6, the fringe field between the gate (comb finger) edge and GP1, GP2 also results in an overall change in the field experienced by the JLFET channel, as shown in figure 7. Here, it can be seen that the fringe field enclosing the area between the edge $\overline{dg}$ and terminating onto the GP1 edge $\overline{UY}$ undergoes a change as ΔZ varies from 0 to 2nm. By virtue of symmetry, this is true for edges ch and the corresponding edge on GP2. Also, the corner fringe arising out of the gate corner points c, d and terminating on GP1, GP2 respectively would exhibit variation as ΔZ varies from 0 to 2nm along the +ve Z-direction.

The resulting fringe field variation as a result of the discussion above reduces the pinch-off voltage (V_p) of the JLFET as ΔZ varies from 0 to 2nm.

This reduction in the pinch-off voltage V_p) for a change in the gate displacement brings about a parallel shift in the Log (I_{DS}-V_{GS}) curve. For a chosen DC bias point (V_{GS}) this would bring about a modulation in the drain current (I_{DS}) of the JLFET. Figure 6 illustrates different capacitance components. C_{nr} is the fringe field capacitance originating from the gate displaced face (i.e., when ΔZ =2nm). C_{cr} is the fringe field capacitance due to corner effects as a result of the reduced overlap area. We estimate the total capacitance by converting non-focal electric field lines to confocal field lines [A. Bansal et al., 2005].

$$C_{cr} = K\epsilon_{di}L'\pi^{-1}ln\frac{\pi L'}{\sqrt{((G_{gap}^2)+\Delta Z^2)}}e^{-(G_{gap}-\Delta Z)/(G_{gap}+\Delta Z)} \quad (1)$$

$$C_{nr} = \frac{2\epsilon_{di}}{\pi}L'ln[\frac{\eta\Delta Z+\sqrt{((G_{gap})^2+(\eta\Delta Z)^2)}}{G_{gap}}] \quad (2)$$

$$C_{fr} = C_{cr} + C_{nr} \quad (3)$$

$$C_{Total} = C_{fr} + C_{Ovrlap} + C_{par} \quad (4)$$

Here C_{cr} is the fringe capacitance due to corner effects and C_{nr} is the fringe capacitance due to normal field as in figure 6. C_{par} is the parasitic capacitance contributed by static parallel plate capacitances between the gate, GP1 and GP2. C_{ovrlap} is the overlap capacitance between the gate electrode and the channel. K is an empirical constant (K = 0.1 [Bansal et al., 2005] and is arrived at by referencing with TCAD simulated data), physical channel length L = 50nm, L' is the approximated gate length with field termination onto GP1 & GP2 (i.e., e to j distance & k to f distance as in figure 7), L'= L/2 = 25nm, G_{gap} = distance between the gate and the channel spacing = 105nm, gate displacement ΔZ = 2nm. Table I shows an estimate of the capacitance values for ΔZ = 0 and ΔZ = 2nm. For fringe capacitance calculation only the comb fingertip surface bounded by edges $\overline{abcd}$ in figure 7 is considered. (Note that in figure 7, the edge $\overline{dgilhc}$ is in the same plane as that of the edge $\overline{XYU}$ when ΔZ = 0). $\overline{aegd}$ and $\overline{bchf}$ are the overlap areas

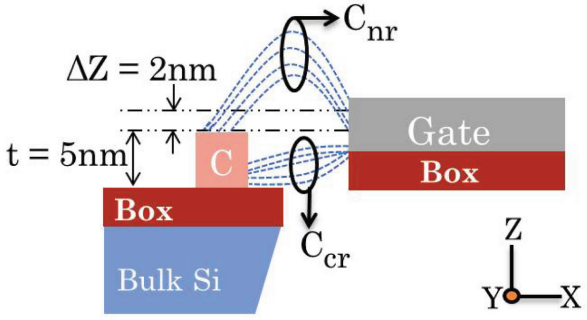
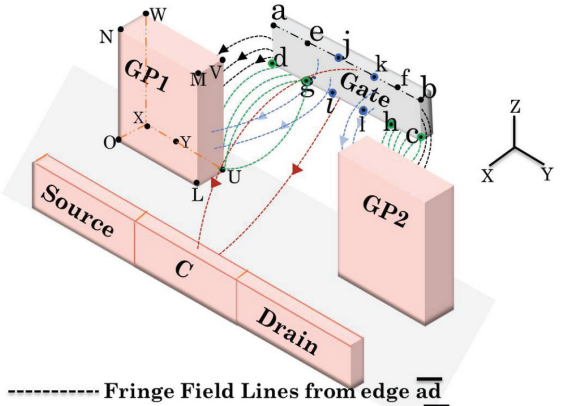


Fig. 6 Fringe Field lines compensating for reduced physical overlap area.



Fringe Field Lines from edge $\overline{ad}$
Fringe Field Lines from edge $\overline{dg}$
Fringe Field Lines from gate center onto the GP1 sidewall $\overline{UVML}$
Fringe Field Lines from gate top edge $\overline{jk}$ and bottom edge $\overline{il}$ onto JLFET Channel

Fig.7 3D View of the Fringe Field lines arising from different gate (comb finger) edges and corner points

of the gate with GP1 & GP2. Surface efhg is the overlap area of the gate with Channel (C) of the JLFET. The fringe field lines arising out of the edge $\overline{ad}$ and $\overline{bc}$ contribute to the static parasitic capacitance, whereas the corner points 'c' and 'd' contribute to the dynamic fringe capacitance when the gate moves from $\Delta Z = 0$ to $\Delta Z = 2nm$. The corner point 'g' contributes to the fringe in the GP1 sidewall ($\overline{UVML}$). Although the surface bounded by $\overline{efgh}$ overlaps with the JLFET channel, the actual gate surface considered for parallel plate estimation is the surface bounded by $\overline{jkil}$. In other words the actual gate length considered for analytical purposes is L' = L / 2). This is because the field arising from the surfaces bounded by edges $\overline{ejgi}$ and $\overline{kfhl}$ have GP1 & GP2 as closer field termination points respectively. This is the approximation carried out in the analytical model. The length between points 'j' & 'k' hence is 25nm. The length between points 'e' & 'j' is 12.5nm. The fringe field arising out of the edge $\overline{gi}$ and terminating on $\overline{LU}$ contributes to the dynamic corner fringe capacitance (C_{cr}). The dynamic fringe capacitance arising from the surface bounded by $\overline{ejgi}$ and terminating on GP1 is classified under the normal fringe capacitance (C_{nr}) as the gate displaces from $\Delta Z = 0$ to $\Delta Z = 2nm$. The cumulative capacitances estimated analytically considering all the afore mentioned surfaces / edges and their corresponding normal fringe capacitance components and corner fringe capacitance components is summarized in Table I. For different fringe components the G_{gap} takes values as 105nm or 50nm. For instance, while estimating the fringe capacitance between Gate and GP1 or GP2, G_{gap} is 50nm. While estimating the fringe capacitance between Gate and the JLFET Channel G_{gap} is 105nm.

Table I: Total capacitance estimate arising out of the fringe field

ΔZ	C_{par}	C_{fr}	C_{Ovrlap}	C_{Total}
0	28.3zF	-	10.5zF	39zF
2nm	28.3zF	13.4zF	6zF	48.1zF
				ΔC = 9.1zF

It can be noted that the static parasitic capacitance is 28.3 zF in both cases. Although the overlap capacitance when $\Delta Z = 2nm$ is lower than the capacitance when $\Delta Z = 0$ (due to a reduction in the physical overlap area), the extra dynamic fringe capacitance (C_{fr}) which is 13.4zF when $\Delta Z = 2nm$ makes up for the reduction in the physical overlap area. Hence, the C_{Total} in the case of $\Delta Z = 2nm$ is higher than when $\Delta Z = 0$ by a magnitude of 9.1zF. This indicates that the gate exerts better control on the JLFET channel despite a physical reduction in overlap area due to the dynamic fringe contribution when $\Delta Z = 2nm$. This enhanced coupling effect between the gate and the channel indeed gives rise to a reduction in the drain current (I_D) as demonstrated by 3D TCAD simulations in the following section. Note that better gate coupling (by the dynamic fringe component C_{fr} depletes the channel, with a lower gate voltage leading to a reduction in I_D. The reduction in I_D which we observe through TCAD simulations (seen subsequently in section IV) for $\Delta Z = 2nm$ is attributed to the above reason.

The FF-JLFET principle we propose is different from [Song and Ajmera, 2009][Grogg et al., 2011] on four counts:

- The JLFET body is static and the gate is displaced. Further the displacement in our proposal is out of plane and not lateral as in [Grogg et al., 2011].
- The NEMs gate interfaced onto the JLFET is a comb drive which maintains a fixed gap with the JLFET channel during the course of operation. This overcomes the pull-in constraint.
- The JLFET has predefined Ground Planes (GP1 and GP2) to terminate the extra fringe field outside the channel zone and to participate in the modulation of the fringe field which the JLFET channel (C) experiences.
- The fringe field difference arising due to the out-of-plane gate movement brings about a change in the JLFET I_{DS}-V_{GS} characteristics for a chosen bias point (V_{GS}). The sensitivity offered due to this change is the primary merit of this proposed transduction.

5. 3D TCAD Simulation

The FF-JLFET device simulated in the TCAD environment [TCAD Manual] is as shown in figure 3. The NEMs/ MEMs comb finger is coupled onto the FF-JLFET. We use the Synopsys Sentaurus TCAD tool for simulations.

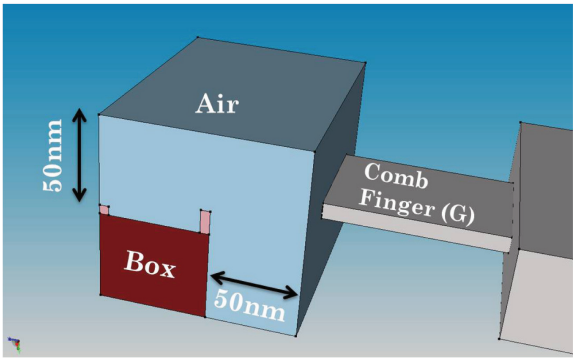


Fig. 8 Isometric view of the FF-JLFET in a TCAD environment with surrounding air acting as the fringe space

5.1. Effect of Ground Plane Spacing on Sensitivity

Figure 8 shows the fringe space extended in the positive Z-direction (in the form of material Air) to study the effect of the fringing field surrounding the FF-JLFET. The I_{DS}-V_{GS} sweep was simulated considering V_{DS} = +2V and the ground planes (GP1 and GP2) are biased at 0V. The work function of the gate material considered for simulation purposes was 5.5eV. A change in the work function of the gate material offers a fixed shift in the pinch-off voltage of the JLFET but has no impact on the device sensitivity. Figure 9 depicts the output characteristics of FF-JLFET in response to two different gate displacements ΔZ = 0 (i.e., no gate displacement) and ΔZ = 2nm. We also show here the I_{DS}-V_{GS} characteristics obtained with and without the ground planes (GP) for $N_D = 8X10^{16}cm^{-3}$. The effect of Ground planes on the JLFET characteristics is seen clearly.

In the absence of GP1 and GP2 (i.e., without GP) the sub-threshold slope factor is nearly 600 mV/dec, and in the presence of GP1 and GP2, the sub-threshold slope factor degrades to nearly 2 V/ dec. This is due to the ground plane acting as a field sink. However, the presence of the GP, ensures that the fringe field plays an important role and gives

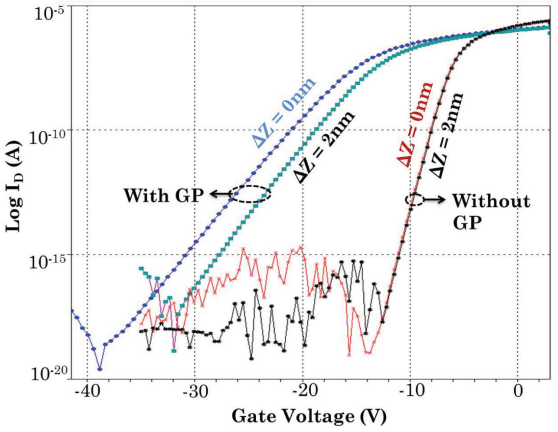


Fig. 9 3D TCAD simulations to determine the influence of Ground Planes (GP) on the JLFET I_{DS}-V_{GS} characteristics. Here $N_D = 8X10^{16}Cm^{-3}$

rise to a change $\Delta I_D/I_D$ for a shift ΔZ = 2nm. Figure 10 highlights the effect of varied channel doping concentrations on the output characteristics of the FF-JLFET. The I_{DS}-V_{GS} curves with ΔZ = 0 & 2nm tend to become distinctly separate with higher channel doping. This is because as the doping is increased the channel resistance drops thus providing a better field termination path for the field lines which go past the GP1 & GP2. Thus, when the doping $N_D = 8X10^{16}cm^{-3}$ at bias point V_G = -21V, the sensitivity defined as $\Delta I_D / I_D$ is 50%. On the other hand, for the doping $N_D = 8X10^{18}cm^{-3}$ at bias point V_G = - 47.7V, the change in current magnitude is by about 2 orders i.e., 98% sensitivity.

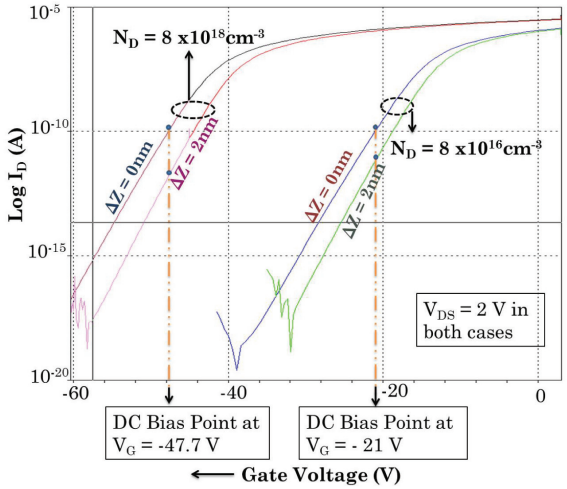


Fig. 10 Influence of channel doping on sensitivity. At a bias point of - 47.7 V the change in current magnitude is about 2 orders (98%) for 2nm gate displacement. For lower channel doping and a bias of -21V the change in current magnitude is nearly 0.5 orders (50%) for 2nm.

The change in the drain current as seen from figure 10 is negative, meaning the drain current drops from 10^{-10} to 10^{-12} for a gate displacement of 2nm. This implies that a change in the gate displacement ensures higher field coupling thus lowering the pinch-off voltage (V_P).

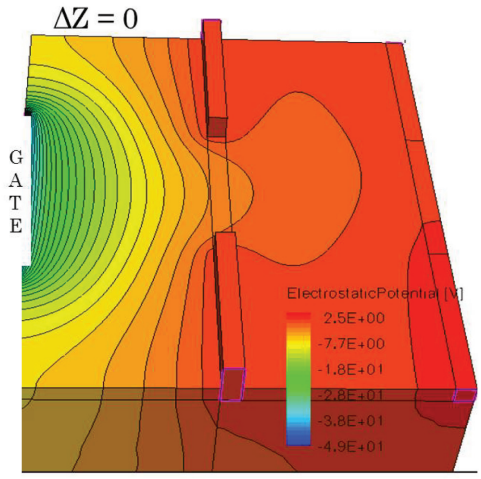


Fig. 11 Equipotential lines for gate displacement ΔZ = 0. Here N_D= 8X10^{18}cm^{-3} and bias point V_G = - 47.7 V, V_{DS} = 2 V. (The top fringe space marked as 'Air' in figure 8 is intentionally hidden in this view).

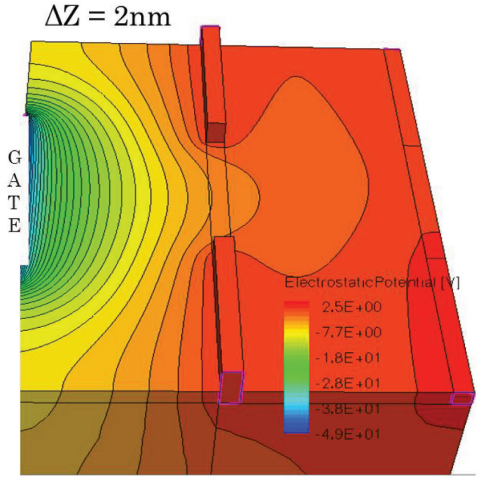


Fig. 12 Equipotential lines for gate displacement ΔZ = 2nm. Here N_D= 8X10^{18}cm^{-3} and bias point V_G= - 47.7 V, V_{DS} = 2 V. (The top fringe space marked as 'Air' in figure 8 is intentionally hidden in this view)

Figure 11 shows the representative equipotential lines originating from the gate and terminating on GP1, GP2 and source/drain regions when ΔZ = 0. Figure 12 shows the equipotential lines having a higher penetration depth when the gate displacement ΔZ = 2nm in the positive Z-direction. This illustrates better coupling between the gate and the channel when ΔZ = 2nm as compared with the case when ΔZ = 0.

The effect of variation in spacing between two ground planes (i.e., GP1 and GP2) on the sensitivity factor of the FF-JLFET is shown in figure 13. The sensitivity shows an increasing trend as the GP Spacing (GPS) begins to widen up to 50nm. The sensitivity peaks at 50nm of GPS since this corresponds to uncovering the entire channel length (L = 50nm). Once the GP spacing increases beyond 50nm, the source of the JLFET is also uncovered and the role of GP almost disappears. As can also be observed from figure 14, the reduction in GPS prevents the gate field from reaching the channel causing the pinch-off voltage to rise. The pinch-off voltage of the FF-JLFET is a design trade-off parameter since it is a strong function of GP spacing.

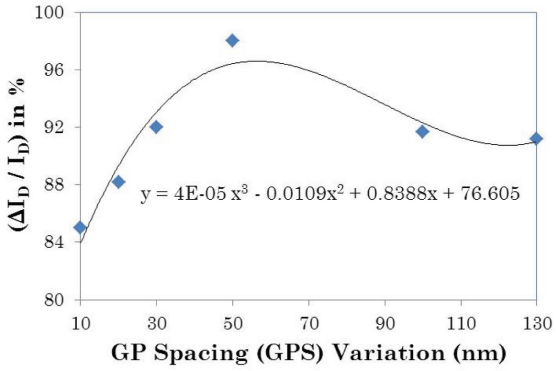


Fig. 13 Variation in Ground Plane spacing (GPS) and its impact on FF-JLFET sensitivity. Here N_D = 8X10^{18}cm^{-3} and the GPS is varied from 10nm to 130nm.

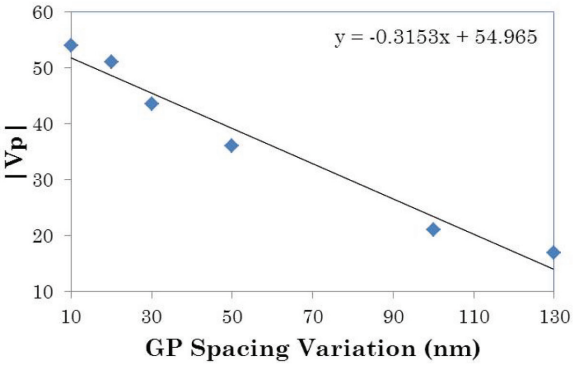


Fig. 14 Variation in Ground Plane Spacing (GPS) and its impact on FF-JLFET Pinch-off Voltage. Here N_D= 8X10^{18}cm^{-3} and the GPS is varied from 10nm to 130nm.

In order to further ascertain the extent of the effect of ΔZ on the coupling between the gate and

the channel, the resulting capacitance variation for a displacement of 2nm is estimated from the total space charge of the channel considering a fixed GP spacing of 50nm and N_D = 8X10^{18} cm^{-3}. The channel space charge as a function of the gate voltage is plotted in Figure 15. For positive gate voltages the channel is in strong accumulation, since the JLFET has n^+-n^--n^+ as the doping profile for source-channel-drain respectively. The channel potential as a function of the gate voltage is also shown in figure 15.

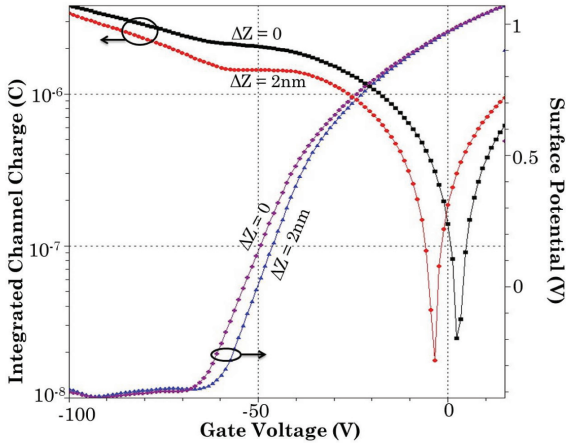


Fig. 15 Channel Charge (integrated) variation as a function of the Gate voltage, estimated from TCAD simulation

It can be observed that the slope of the channel potential is very poor in the presence of ground planes which shield the field from reaching onto the channel. The slope degradation and an increase in the pinch-off voltage is also observed in the current plot figure 9 for case when N_D = 8X10^{16}cm^{-3}. The significant degradation in the channel potential is due to the presence of ground planes which shields the field from encroaching onto the channel. As the gate voltage is decreased from a positive value to negative value, the channel charge begins to drop, reaches a minimum at flat band followed by depletion of carriers and eventually transitions to the weak and strong inversion regimes. The charge plot seen in figure 15, is the 3D integrated channel charge i.e., q (p - n + N_A - N_D). This integrated charge does not account for the overall charge present on the gate since the capacitive equivalent of the FF-JLFET is as in figure 16.

Here C_{sc} is the source channel capacitance of the JLFET. C_{GP1} and C_{GP2} are the gate to GP1 and gate to GP2 capacitances respectively. C_{Gap} is the air gap capacitance between the gate and the channel.

The overall gate charge (Q_G) seen at the gate terminal comprises charge summation at the other 4 contact terminals namely GP1, GP2, Source and Drain.

The influence of drain is nearly absent as there are no short channel effects in JLFET due to common dopant species.

$$Q_G = |Q_{GP1}| + |Q_{GP2}| + |Q_S| + |Q_D| \quad (5)$$

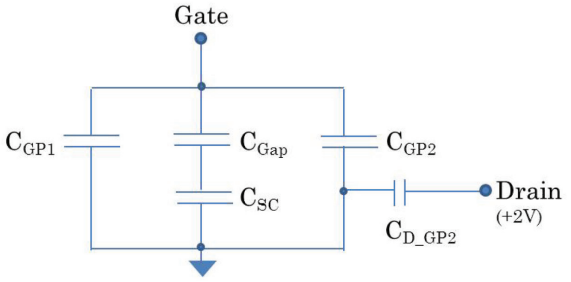


Fig. 16 Capative Equivalent of FF-JLFET

With the above relation, Q_G at the gate terminal is evaluated for cases when the gate displacement ΔZ = 0 and ΔZ = 2nm. The near linear relation of the gate charge as a function of the gate voltage is shown in figure 17.

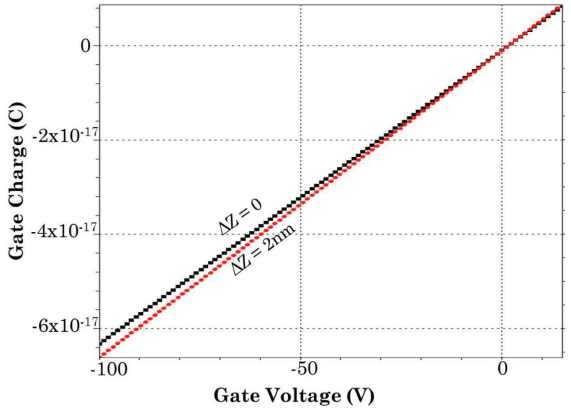


Fig. 17 Total Charge at the Gate terminal as extracted from TCAD 3D simulations

The near linear variation in Q_G is due to the presence of parasitic capacitances (C_{GP1} and C_{GP2}) and due to the poor gate to JLFET channel coupling (since the air gap is 105nm). The parallel and fringe capacitances dominate the JLFET channel capacitance resulting in a deviation of the gate charge behavior as per the JLFET theory [Colinge et al., 2010]. In a conventional JLFET, the gate charge and channel charge track each other with an opposite sign convention. In the FF-JLFET the gate charge is different from the channel charge as seen from figure 15 & figure 16.

Table-2: Gate capacitance estimate from total gate charge

ΔZ	$\|Q_G\|$	$C = Q_G / V$
0	$3.0766x\ 10^{-17}$	645zF
2nm	$3.215x10^{-17}$	674zF
		ΔC = 29zF

This capacitance metric is extracted from the gate charge for a case when ΔZ = 0 and when ΔZ = 2nm at a bias point of - 47.7 V. The difference in the resulting capacitances from figure 17 is 29 zF. It is seen that the extracted value of capacitance from the 3D TCAD simulations (as in Table II) and the value of the capacitance calculated analytically (listed in Table I using equations (1)-(4)) differs by a factor of 3, but is in the same order (i.e., in Zepto Farad). The variation seen in the capacitance estimated through TCAD 3D simulations and that estimated through the analytical approach is likely due to 2D approximation in the analytical model [Bansal et al., 2005].

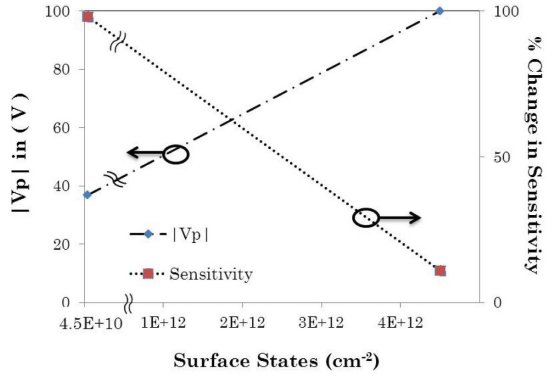


Fig. 18 Impact of surface states on the JLFET characteristics namely pinch off and sensitivity

5.2 Effect of Interface Trap Density N_{it} on Sensitivity

The effect of the interface traps present at the BOX-silicon interface was simulated to ascertain its impact on the sensitivity factor of the FF-JLFET. The interface trap densities N_{it} considered were $4.5X10^{10}cm^{-2}eV^{-1}$. TCAD simulation shows a reduction in the pinch-off voltage in the presence of interface traps by about 300mV but the sensitivity of the FF-JLFET as such, remained unaffected. The impact of the surface states present on the other sides of the silicon surface (excluding the box side) was ascertained through TCAD simulations. A surface state density of the order of $4.5X10^{10}cm^{-2}eV^{-1}$ and $4.5X10^{12}cm^{-2}eV^{-1}$ was considered. GP spacing is kept constant at 50nm and $N_D = 8X10^{18}cm^{-3}$ in this analysis. It was observed that, the $|V_P|$ increases by about 900mV (from the earlier value seen in figure 14) for a surface state density of $4.5X10^{10}cm^{-2}eV^{-1}$.

The variation in V_P is evaluated for the higher surface state condition $4.5X10^{12}cm^{-2}eV^{-1}$. In this case, it can be seen that the $|V_P|$ increases significantly and the sensitivity factor drops to 11%, the results of which are shown in figure 18. The surface states thus significantly influence the pinch-off voltage and sensitivity parameters of the FF-JLFET, in case the silicon surface is not well passivated. Hence, it is proposed to have a thin layer of silicon-dioxide of 1nm thickness on the JLFET channel to minimize the interface charge effect on the performance parameters of the FF-JLFET. The sensitivity of the FF-JLFET could be restored by this slight modification in the device structure.

As per the Paschen curve [Paschen 2013], for an air gap of 105nm (gap between gate and channel) and a pressure of 760 Torr, the dielectric breakdown is > 100kV which is significantly higher than the FF-JLFET operation range. The mean free path for gas phase collisions at 760 Torr is 65nm with the likely hood; of at least one collision in the 105nm gap mentioned. Since the air gap between the gate and the channel of the FF-JLFET is 105nm and the proposed bias point for a channel doping of $8x10^{18}cm^{-3}$ is - 47.7V, the corresponding electric field is 4.5 MV/cm which is much lower than the typical electric field of 8-10MV/cm required for field emission. Hence, the effect of field emission is not

Table-3 Comparison of performance metrics

	Ref [Song and Ajmera 2009]	Ref [Langfelder et al., 2011]	This Work
Sensing Principle	Lateral Gate FET	Fringe Based Capacitance Sense	Fringe Induced I_D Modulation
Sensitivity	1.4% change in current	5% change in capacitance	98% change in current
Dynamic Range	±30μm	±4μm	±5nm (extendable)
Pull-in Constraint	Not Present	Not Present	Not Present
Cross axis	NA	<1%	No impact upto 10nm variation in-plane

considered for the purpose of analysis in this paper.

The results of the proposed FF-JLFET transduction principle are summarized with the reported literature metrics on displacement sensing in Table III. It is seen that the FF-JLFET offers much higher sensitivity than those reported in references employing built-in transduction methodology. The dynamic range of the FF-JLFET

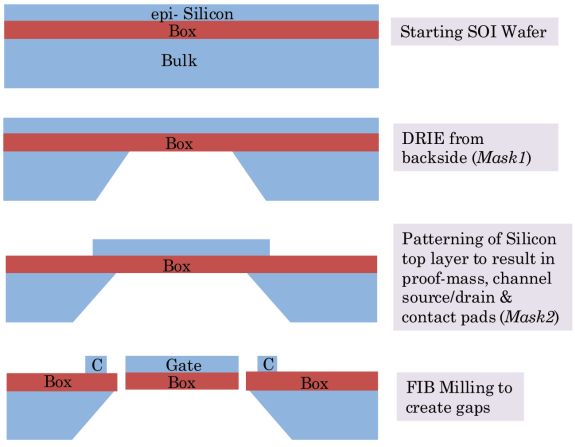


Fig. 19 Fabrication Process Flow of FF-JLFET in crossection. (Top View of FF-JLFET as in figure.2)

is marked as extendable since the initial thickness of the device can be increased based on the initial SOI wafer of choice. The out-of-plane gate (comb drive) displacement maintaining a fixed distance with respect to the JLFET channel, eliminates the pull-in effect.

The cross-axis margin of the FF-JLFET is 10nm and is arrived at as follows: The sense axis for the proposed device is along the z-axis and the cross-axis in the device proposed is along the y-axis (i.e., lateral direction as in figure-7). and are the overlap areas of the gate with respect to ground planes GP1 and GP2. and have overlap lengths of 10nm with respect to GP1 and GP2 respectively. In case the gate gets displaced along the y-axis (which amounts to a cross-axis deflection), the effective overlap area increases with and GP1 and there would be a corresponding reduction of effective overlap area along and GP2. Due to the extra initial overlap of 10nm between and GP1 on the one side and and GP2 on the other side of the gate in figure.7, the maximum cross-axis margin is 10nm.

6. Fabrication Steps for FF-JLFET

The proposed FF-JLFET device is on a SOI substrate with the key fabrication process steps summarized in figure. 19.

7. Conclusions

A new transduction methodology based on fringe field sensing to detect nano meter displacements of less than 5nm is proposed. The novel sensing scheme brings about nearly 2-orders of magnitude change in the drain current for a 2nm change in displacement. The ground plane spacing and its influence on the fringe field is analyzed. The effect of doping concentrations on the sensitivity aspect is highlighted. The trade-off factor in terms of channel pinch off and biasing is presented. For channel doping of $8X10^{18}cm^{-3}$ and a bias point of - 47.7V, the FF-JLFET offers 98% sensitivity offering the best sensitivity of 98% for a GP spacing of 50nm. The influence of the surface states on the pinch off voltage and sensitivity is highlighted for the best and the worst case scenarios

considering $4.5X10^{10}cm^{-2}eV^{-1}$ and $4.5X10^{12}cm^{-2}eV^{-1}$ respectively. Surface passivation to mitigate the influence of surface states, by growing a 1nm silicon oxide on the channel surface of JLFET is proposed in the final device architecture. The proposed transduction methodology is compared with state-of-art principles and is shown to be promising based on TCAD 3D simulations. The proposed technique is shown to measure an equivalent of 29 zF change in capacitance as extracted from the TCAD gate charge (Q_G) estimate, when biased in the above-pinch-off ($> |V_P|$) regime.

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