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A newsletter about micro and smart systems in India

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CONTENTS

Small Steps in the World of the Small — Editorial

With this issue, Sukshma completes two years since its birth in October, 2006. It is taking small steps with its modest eight pages in each issue, like a toddler learning to walk and aspiring to run. An important intent of Sukshma, besides being a medium to inform the world about the activities of the Institute of Smart Structures and Systems (ISSS), is to highlight the research, events, people and institutions, and the human resource development activities in the micro, nano, and smart technologies that are growing at a fast pace in India. The interdisciplinary nature of these areas is bringing together people working in different fields. Furthermore, with the impetus given by these technologies of the small and smart, the academia, government research labs, and the industry are getting intertwined more and more in the so-called triple helix of the modern research invironment. Sukshma is trying to do its part in informing its readers about the role of the different players contributing to this effort in India. And there is a lot more to do because we anticipate that the interest in these areas will be on the rise in years to come. We request the readers to contribute articles to Sukshma. There are many avenues to contribute. Some are noted below. We also seek your feedback and suggestions for improvement. Please contact us by sending an e-mail to **sukshma@mecheng.iisc.ernet.in.**

Ten ways to contribute to Sukshma

(1) Did you attend a workshop, seminar, or a conference in the areas of micro, nano, or smart (MNS) technologies in India? Write a brief note about it with a picture or two.

(2) Did you come across an Indian industry, small or big, that is enganged in the MNS areas? Send us a brief write-up for the "Industry Watch" column.

3) Do you want to write a tutorial-style article on an MNS topic of your expertise? Send it for the centre-spread that occupies two pages in every issue of Sukshma.

(4) Is your institution engaged in education and research in the MNS areas? Send a brief article and a picture or two for the "University Buzz" and "Accomplishments" columns.

(5) Did you just read about some latest news in the MNS areas? Send it to us for the "Technology News" column.

(6) You can write a book review for a recent book that you have come across in the MNS area.

(7) If you wish to announce a call for papers for a conference or about a seminar or workshop in the MNS areas, you can do so in Sukshma.

(8) If you are a company, you can also advertise in Sukshma.

(9) Any other technical contribution will be appreciated. (10) Finally, please give us feedback on what you like or do not like in Sukshma.

Smart Technologies for a New Generation RTA — Kota Harinarayana

The Indian civil aviation industry has seen unprecedented expansion of the economy, introduction of low cost airlines, and increase in disposable incomes across the country. A number of small towns and cities have been connected by carriers such as Deccan using regional aircraft. However, viability of the airlines has been affected by the high ownership costs of aircraft, maintenance costs, and exceedingly high fuel costs. Across the world, airlines are now dependent on high efficiencies that have to be obtained from innovative design of materials and systems. National Aerospace Laboratories (NAL), Bangalore, which has a focus on civil aircraft design and development, is presently working on a new generation regional transport aircraft (RTA) that is envisaged to have at least 25% lower ownership and fuel costs apart from 50% less maintenance costs over present generation aircraft.

A concept sketch of RTA-70, a regional transport aircraft being developed by NAL, Bangalore.

To achieve this, the aim is to develop technologies such as laminar flow aerodynamics, super hydrophobic coatings to maintain the laminar flow, fly-by-wire, low cost composites, structural health monitoring and integrated vehicle health management, and enhanced synthetic vision to land in ill-equipped airfields in all-weather conditions. Importantly, the aircraft design is being considered using an all-electric architecture that reduces engine bleed off-take. There appear exciting possibilities of using devices for monitoring and control in all these new technology areas. Specifically, we see application in aerodynamics, structural vibrations control, noise control, and health monitoring. Furthermore, given that there are numerous sub-systems in an aircraft which are maintenance-intensive, these systems could benefit from smart materials and devices in bringing down maintenance costs and increasing reliability.

Dr. Kota Harinarayana is currently the Raja Ramanna Fellow at the National Aerospace Laboratories (NAL) in Bangalore. He is leading the effort in the development of RTA-70.

Piezo-ceramic seminar in NAL

A one-day seminar on piezo-ceramic materials, actuators, and sensors was held in the National Aerospace Laboratories (NAL), Bangalore, on 21st June, 2008. The purpose of this seminar was to highlight the activities of NAL in this area and bring together researchers from other organizations who are working in this area. Dr. A.R. Upadhya, Director of NAL, welcomed the audience and chaired the first session on modeling, analysis, design, and applications. The talks in this session were given by Dr. K. Vijayaraju of Aeronautical Development Agency (*Applications of piezo materials in aero structures*), prof. S. Gopalakrishnan of IISc (*Comparison of actuator authority of piezoelectric and electrostrictive actuators*), and Prof. D. Roy Mahapatra of IISc (*Modeling, analysis, and design of piezoelectric materials and devices for smart structural applications*). The second session, which was chaired by Prof. S. Gopalakrishnan, consisted of three talks by Dr. P.K. Panda of NAL (*Development of piezo-ceramic materials and devices at NAL*), Prof. G.K. Ananthasuresh of IISc (*Enhancing the performance of piezo-actuators with mechanical amplification*), Dr. Roderick Hoppener of Haiku Tech. Inc. (*Novel piezo-actuators for large displacements by tape casting technique*), and Dr. A Madhusoodan Rao of ISAC, ISRO (*Multi-layered ceramic capacitors for space applications*). There was also a third session chaired by Dr. K. Vijayaraju that consisted of four more talks by Dr. S. Raja (*Applications of piezoelectric materials and devices in aerospace structures: perspectives*), Dr. Shashikala Prakash (*Use of piezoelectric sensors/actuators for active vibration control of aircraft*), Dr. Ranjan Moodithaya (*High-frequency applications of piezo-actuators*), and Dr. G. Ramesh (*Development of smart actuators for boundary layer separation and control*). The seminar ended with a panel discussion. More information about this seminar can be obtained by contacting Dr. P.K. Panda at pkpanda@css.nal.res.in.

ISSS 2008 Conference Update — Organising and Technical Committees

Various organizational and technical activities are in full swing in preparation for the ISSS 2008 International Conference on Smart Materials, Structures, and Systems. Under the leadership of the Conference Co-chairs, Dr. P.S. Nair and Prof. S. Gopalakrishnan, different committees are working to ensure that the conference, which will be held from July 24-26, 2008 in the National Science Seminar Complex of the Indian Institute of Science, Banaglore, runs smoothly. The technical committee, co-chaired by Prof. Rudra Pratap and Prof. G.K. Ananthasuresh and consisting of many members (Prof. Navakanta Bhat, Prof. K.J. Vinoy, Dr. G.M. Kamath, Prof. T. Srinivas, Prof. D. Roy Mahapatra, Prof. Kartik Venkataraman, Dr. M. M. Nayak, Dr. A. K. Sharma, Dr. K. Vijayaraju, Prof. Ranjan Ganguli, Prof. V. Venkataraman, and Dr. C.L. Nagendra) has completed the task of full paper review. The conference organisers thank the authors for submitting the full papers and the reviewers who generously devoted their time to review the papers. The review was conducted partly online (www.isss.in) and partly via e-mail. Based on the reviewers' recommendations, 64 papers were accepted for oral presentation and 18 for poster presentation. Eight papers were rejected. Poster presentations will be given a prominent time-slot during the conference to facilitate dedicated time of the full audience (as opposed to parallel oral sessions) and lively interaction between authors and conference attendees. The conference will have five plenary talks and more than 20 invited talks in addition to the above contributed papers.

There will be two workshops prior to the conference on July 23rd, 2008 on structural health monitoring and photonics. The ISSS members are encouraged to register early for the conference and the workshops.

Register for the ISSS 2008 conference at http://www.isss.in/registration.html

ISSS News — S. Gopalakrishnan

The governing council of ISSS is discussing and preparing the by-laws for the chapter formation. ISSS currently has two chapters, one in Hyderabad and the other in New Delhi. More chapters are likely to be formed in the coming years to spread the activities of ISSS throughout the nation. Professor Dattaguru (see Vol. 2, No. 1, p. 3) is going to organize an International Union of Theoretical and Applied Mechanics (IUTAM) symposium on multifunctional materials and systems during December 10-12, 2008 in Bangalore. ISSS will be co-sponsoring this event, which consists of only invited speakers from around the world. The council has decided that it will partially fund three conferences per year and will partially support the travel of three scientists/students to attend conferences per year. The annual general-body meeting (AGM) of ISSS will be held during the ISSS 2008 International Conference on Smart Materials, Structures, and Systems to be held from July 24th to 26th, 2008 in the National Science Seminar Complex, Indian Institute of Science, Bangalore. ISSS thanks all the authors, invited speakers, and reviewers for their enthusiastic support in submitting and reviewing papers submitted to this conference. ISSS also thanks various committees that are tirelessly working to make this conference a success.

Industry Watch: World Micromachine Summit 2008

V.K. Aatre

The 14th World Micromachine Summit 2008 (*http://www.micromachinesummit.org/*) was held in Daejeon, Republic of Korea (30th April to 3rd May). Founded by Mr. Hirano of Japan, the Summit meets every year. The next year's meet will be held in Canada. 18 countries with 56 delegates and 43 observers participated in the present Summit which had the thematic subject 'Micro Machines towards Technology Convergence era'. Following the presentation of delegates which covered the activities, policies and strategies of the respective country/regions, microscopic features of several subtopics - technology convergence, technology advances, market, standardization and industrialization, education and technology platforms, and foundry and cluster network - were also presented and discussed. While activities on MEMS and microsystems were the focus of the Summit, Nano technology received considerable attention with the present and future of MNT (micro-nano-technology), manufacturing, and specific applications in biomedicine also being discussed. The main and interesting feature of the Summit was the participation by industries who are deeply involved in MNT. The Summit also brought out the following:

- § MNT is a very highly application oriented technology with tremendous market potential;
- § Clusters formation and joint R&D programs, Nation and Region wide programs are a rule rather exception;
- § Most countries are investing very large amount of funds in the MNT and most of these come from their respective governments;
- § Large industrial participation and hence heavy product orientation;
- § Time-to-market plays a crucial role in the success of a product;
- § Human resource development is receiving considerable attention with large involvement in R&D at both academic and industrial institutions.

The delegates from India – four of us – presented the scenario in India and the recent National Initiatives. Our attending the Summit (and a few other similar ones) put our efforts, in my opinion, in proper perspective.

While we have done well in mounting such initiatives, our efforts are yet to provide any tangible results. While intellectually we are certainly capable of producing the kind of results that have been presented in such and other international gatherings and if we are serious about playing a substantial role in such high-end technologies, we need a paradigm shift is our approach and mindset. In my opinion, the following are of some of the considerations that are crucial to our success and achieving the results we are capable of:

- § The funding for such high technology development and (preliminary) conversion to products must necessarily come from the government;
- § Our resources allocation both in terms of funding and manpower is sub-critical and insufficient to make any impact in the world technological scenario;
- § Active Industrial participation in the development and technology conversion to product is not only essential but crucial to the success of any initiative;
- § Time to market being the *coup de grace*, we have to show certain urgency in R&D and productisation which seems to be essentially missing in most of our developmental work;
- § Academic Institutions and Industries must consider the technology and product development as joint responsibility, albeit in different proportions. Academic Institutions cannot abdicate from the responsibility of product development and Industries cannot be by-standers in the development.

May be I am not saying anything new. But with a large percentage of our population being below 35 years of age and the intelligence and creativity of such young Indians making waves elsewhere in the world, it is time to once again ponder over the local scenario in Science & Technology and make necessary changes in the policy and practices.

Dr. V.K. Aatre, the former Scientific Adviser to the Raksha Manthri, is currently a visiting professor in the ECE department in IISc.

Announcements

Indian Society for Advancement of Materials and Process Engineering (ISAMPE) invites nominations for the following awards.

VIJAY ZAVERI AWARD FOR EXCELLENCE IN TECHNICAL SUPPORT IN THE FIELD OF COMPOSITES-2009.

K. SURYANARAIN RAU MEMORIAL JUNIOR and SENIOR STUDENT AWARD" for "RESEARCH AND DEVELOPMENT IN SMART TECHNOLOGY

The details can be found at http://www.isampe.org/awards.htm. Completed application/nomination duly signed should be sent to The Secretary, ISAMPE, Aeronautical Society of India Building, Suranjan Das Road, New Thippasandra PO, Bangalore-560 075.

ISSS is pleased to announce that there will be best paper awards in its 2008 International Conference on Smart Materials, Structures, and Systems conference. There will be one best paper award in each of the three categories: (i) Microelectromechanical systems technology, (ii) Smart materials and structures technology, and (iii) micro or smart devices or systems. The shortlist of the candidate papers was drawn based on the full papers submitted for the conference. The reviewers were asked to indicate their recommendations for the best paper award in their reviews. A committee of distinguished judges will be present when these papers are presented during the conference. Based on their evaluation, the awardees will be decided.

Additionally, ISSS is holding a student paper contest. Students were asked to submit a paper based on the research work they did. It was stipulated that all authors be students. Five finalists will be selected to present their papers in a session dedicated for this purpose during the conference. Winners of this student paper contest and the awardees of the best papers will be given certificates of merit and award money in the awards ceremony at the end of the conference. The human resource development PARC of the NP-MaSS (see Vol. 3, No. 1, p. 1) has agreed to sponsor the ISSS conference awards.

In 2006, the Department of Information Technology (DIT), which is a part of the Ministry of Communications & Information Technology (MCIT), launched a major initiative in the country to set up two Centres of Excellence in Nanoelectronics. The Indian Institute of Science (IISc) and the Indian Institute of Technology-Bombay (IIT-B), Mumbai, identified as having the two leading research groups in this area, were chosen as the sites of these centres. These centres undertake state-of-the-art research in nanoelectronics, train manpower in this emerging area, interact with industry and research laboratories, and have created facilities which will be used by nanoelectronics researchers all over the country (*see* Vol. 2, No. 3, p. 1 and p. 7 to learn about the Indian Nanoelectronics User Programme). The two centres, while having common interest in nanoelectronics, focus on complementary activities in materials aspects (IISc) and circuits (IIT-B). Both centres have a broad agenda that encompasses several micro and nano engineering technologies. A highlight of these two centres is that they both will be equipped with the state-of-the-art nanofabrication facilities in India. The birth of the twin nanofabs for India is told in the two articles below.

The Centre for Excellence in Nanoelectronics in IISc

The projected elevation along with the present construction status of the Nano Centre at IISc. The building enabled by a generous funding from the internal resources of the Institute, will have a built up area of 94,000 sft, consisting of lab space, office area, auditorium, and class rooms.

The Indian Institute of Science (IISc) is setting up a comprehensive interdisciplinary centre for nanoscience and nanoengineering. The Centre of Excellence in Nanoelectronics (CEN) at IISc (http://www.nano.iisc.ernet.in), funded by MCIT will be located here. CEN will house a state-of-the-art Nanofabrication facility with 14,000 sft clean room area. The clean room will have a ball room design with functional areas of lithography (with e-beam writer for nanopatterning), plasma etch, wet chemistry, film deposition, thermal process, and in-line characterization. The nanofab will support the realization of a diverse set of devices such as nanotransistors, MEMS/NEMS, sensors on a variety of substrates including Silicon, Germanium, GaAs, Quartz and Glass. The research emphasis will span the entire spectrum of nanomaterials, nanodevices, novel processes, and integrated hybrid systems. The Nanofab will be made available to external users from academia, national labs and industry under Indian Nanoelectronics Users Program (INUP), by 2009. While, the CEN funded by MCIT has acted as a seed for the new building, the interdisciplinary centre will grow beyond this to synergise various other activities in related areas such as nanotechnology projects funded by DST, and several other projects on MEMS/NEMS and smart materials funded by NPSM, DRDO, NPMASS and other funding agencies.

The CEN will be complemented by setting up a comprehensive MEMS/NEMS devices and materials characterization facility, envisioned under the NPMASS. This will be co-located with the Nanofab and will include a comprehensive nano-characterization facility, with an open access for external users. It is also planned to set-up LTCC and Polymer MEMS facilities under NPMASS (*see* Vol. 3, No. 1, p. 1). The National MEMS design centre (NMDC) along with the Computational Nano Engineering (CoNE) centre will be co-located in the same building.

The interdisciplinary centre will also have a provision for additional physical, chemical and bio labs for setting up specific infrastructure. Additionally, four central facilities funded by the Institute, namely XRD facility, Surface Analysis facility, Spectroscopy facility and Imaging facility are likely to be located in the same building.

In summary, the new nano centre at IISc is expected to be one of its kind in the country and will be on par with the best available university facilities worldwide for micro/nano technologies.

Visit
www.nano.iisc.ernet.in
www.ee.iitb.ac.in/~nanoe
for more information.

The Centre for Nanoelectronics setup in the Indian Institute of Technology-Bombay, Mumbai, in collaboration with Applied Materials is shown above in two different views.

Microelectronics has, for many years, been a major area of research at the Indian Institute of Technology-Bombay(IIT-B), Mumbai. The major initiative from the Government of India has, during the past two years, created tremendous interest from industry as well as generated significant support from the Institute itself. The Centre for Excellence in Nanoelectronics in IIT-Bombay, therefore, represents a classic example of a successful government-industry-academia collaboration. This is an opportune time because the semiconductor fabrication industry in India is ready to take off.

The major industry supporter for the Nanoelectronics activities at IIT Bombay has been Applied Materials, Inc., the world's leading semiconductor equipment manufacturer. Applied Materials has endowed the "Applied Materials Nanomanufacturing Laboratory" at IIT Bombay by donating three major high-end semiconductor processing equipment valued at over $ 7.5 million. These are the gate stack cluster tool, capable of depositing various layers (including high-k dielectrics) for a state-of-the-art complementary metal-oxide semiconductor (CMOS) structure, the physical vapour deposition (PVD) deposition cluster tool, and the etch tool. All of these are capable of handling 200 mm wafers. Besides equipment donation, Applied Materials has sponsored several research projects and has participated in a very successful student and faculty / engineer exchange program. Besides Applied Materials, several other global industries, including Intel, Infineon, Renesas, and IBM are partnering with the nanoelectronics faculty for conducting cutting edge research.

The Centre for Excellence in Nanoelectronics at IIT Bombay has a major focus on multi-disciplinary research with a clear emphasis on product development to meet the societal needs. The centre facilities are currently being used by over 25 faculty members and their students from nine different departments and schools at IIT-Bombay. The centre is fast emerging as a hub for inter-departmental interactions at IIT Bombay. A few of the major research projects and initiatives currently underway at the IIT Bombay's Centre for Excellence in Nanoelectronics involving faculty members from multiple departments and schools are summarized in a separate article on page 6 of this issue.

Dr. V. Ramgopal Rao is a professor of Electrical Engineering in the Indian Institute of Technology, Bombay. He can be reached at rrao@ee.iitb.ac.in.

Professor Navakanta Bhat (ECE) and Rudra Pratap (ME) are in the Indian Institute of Science, Bangalore. They can be reached at navakant@ece.iisc.ernet.in and pratap@mecheng.iisc.ernet.in, respectively.

University Buzz: Nano Centre in IIT-B

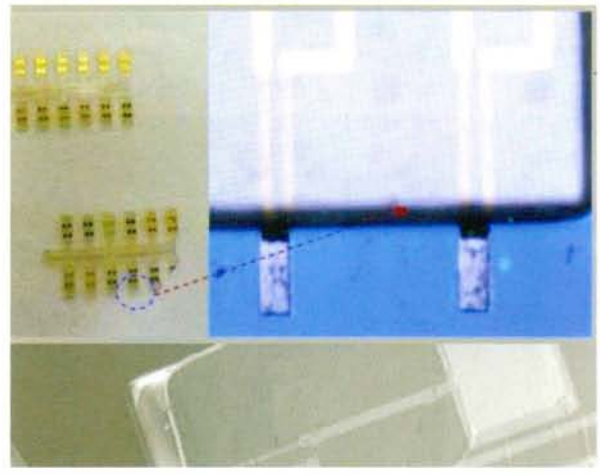
V. Ramgopal Rao

The Indian Institute of Technology, Bombay (IIT-B), is engaged in a number of research activities in its Nanoelectronics Centre involving faculty and students from many departments. Some of these activities are described below. See p. 5 of this issue for a related article.

A Point-of Care System for Cardiac Diagnostics: With an aim to develop a low-cost diagnostic aid for cardiac dysfunctions, the Centre is researching a system that monitors the molecular markers to detect cardiac attacks, especially the incipient cardiac attacks that go undetected before major/fatal attacks occur. The system comprises "infarcSens" or "iSens", which is a cantilever- and molecular field effect transistor (FET) based affinity biosensor array for sensing myocardial infarction and subsequent cardiac status prognosis. A low-cost polymeric cantilever technology with embedded electrical readout schemes has been recently demonstrated in the group with electrical sensitivities in the range of a few ppm per nanometer of deflection, suitable for cardiac marker sensing. The sensing electronics is already in place while the associated data management software for tracking the markers with time, which is required for creating an epidemiological database, is currently being developed. A multidisciplinary team consisting of Prof. V.Ramgopal Rao (EE), Prof. S.Mukherji (BioSchool), Prof. A.Q.Contractor (Chemistry), Prof. R.Lal, Prof. P.R.Apte, Prof. R.Pinto (all EE), and Prof. Prasanna Gandhi (Mechanical Engg) and their students have been working on this project..

Silicon Locket: For mobile monitoring of electrocardiogram (ECG), a small toffee-sized low-cost locket has recently been developed in the Centre by integrating a low power microcomputer with an indigenously developed operating system, analog front-end electronics and a re-chargeable battery with an in-built charger. The system is optimized to acquire a three lead simultaneous ECG reconfigurable up to 12-leads, and to correct for motion artefacts arising out of the physical activity of the patient. The ECG data can be either stored in the Micro SD card memory, or transmitted through a phone modem or GPRS network. An arrhythmia event can be detected in real-time using the built-in algorithms and the system is configured to automatically inform a medical practitioner through SMS in the event of an arrhythmia. The system also allows the doctor to remotely login to the locket to view patient's ECG in real time or download the data using a graphical user interface. The locket is equipped with USB, IrDA and RS232 ports for seamless integration with public networks, mobile phones, and personal computers. An ultra low power custom made analog integrated circuit (IC) is designed and tested which performs all the data acquisition & signal conditioning. A low cost polymeric accelerometer technology developed in the centre is integrated into the electrodes to detect and remove motion artefacts in ambulatory subjects. A pluggable ultra-small PSTN modem is constructed to transfer data to a remote computer or medical database. A 32-bit system-on-chip based base-station is also developed as an accessory for the Silicon Locket. The base station is a handheld system with a higher processing power and a color TFT LCD panel. The base unit primarily has advanced in-built data management and analysis software for ECG analysis. The silicon locket, developed in cooperation with the Tata Consultancy Services, is the smallest wearable ECG recorder in the world, for its features. The technology is currently being transferred to an industry. The contributors to this work have been Prof. D.K.Sharma, Prof. R.Lal, Dr. M.Shojaei (all EE), and Prof. S.Mukherji (Bio-school) and their students.

Disposable Organic Sensors with on-chip Electronics:



Three micron thick polymer cantilevers with embedded nano particles for transduction of deflection.

Also see: www.ee.iitb.ac.in/~nanoe

A group of faculty members from the EE Department (Prof. V.Ramgopal Rao), Chemistry Department (Prof. Anil Kumar, Prof. A.Q.Contractor) and Bioschool (Prof. S.Mukherji) and their students are working closely in the Centre in synthesizing & engineering various organic molecules for specific sensing applications. Using solution processed organic materials, various organic circuits have also been recently demonstrated in the group. By integrating a high-k gate dielectric, low-voltage operation of these sensor circuits is demonstrated using solution processed organic materials. Currently a variety of projects are underway based on this approach.

Bottoms-Up approaches for CMOS Scaling:

The porphyrin self-assembled monolayers (SAMs) engineered for specific applications are currently being explored in the Centre as Cu diffusion barriers and for gate work-function engineering in CMOS, molecular electronics applications as well as for intercalation with DNA to realize a molecular switch with DNA acting as an interconnect. It has also been recently demonstrated that the presence of aromatic rings in a porphyrin core would sterically hinder the Cu diffusion between molecules through the SAM layer and thus making it suitable as a barrier layer for Cu interconnects in ULSI CMOS technologies. This work is being done by Prof.V.Ramgopal Rao, EE; Prof. M.Ravi Kanth and Prof. Anil Kumar, Chemistry; Prof. S.Mukherji, Bio-school; and their students.

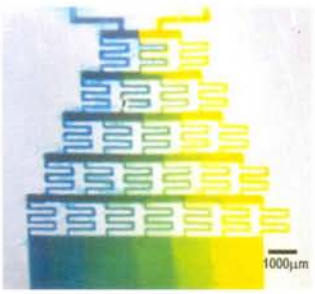
Besides the above activities, there is a significant level of activity in the centre in the area of device design and characterization involving nano-scale devices for logic and memory applications. The group publishes extensively in the world's leading international journals and conferences in these areas.

In summary, the Centre for Excellence in Nanoelectronics at IIT Bombay (initiated as a joint project between IIT-B and IISc) is making rapid strides and significantly contributing to the society and the country in developing the much needed expertise in nanoelectronics in India.

Dr. V. Ramgopal Rao is a professor of Electrical Engineering in the Indian Institute of Technology, Bombay. He can be reached at rrao@ee.iitb.ac.in.

Shrinky Dink® Microfluidics: Childhood Toy Material Meeting Adulthood Research

(Contributed by Vijay Mohan S., BigTec, Bangalore. He can be reached at svijay@bigtec.org)



Gradient generator microchannels made by University of California researchers in Merced and Berkeley using Shrinky Dink moulds and PDMS, and filled with food dye.

Shrinky Dink®, a Children's toy material, has been ingeniously used for microfluidics research by Professor Michelle Khine of University of California, Merced. Shrinky dinks, invented in 1973, are thin, flexible polystyrene plastic sheets that can be cut into shapes and coloured with inks that do not burn or melt. When heated in an oven to about 160 °C, the plastic shrinks biaxially by about 63% and becomes up to nine times thicker and more rigid, while retaining the colored design. Using only a laser jet printer and a toaster oven, Professor Khine's team printed a device layout on a Shrinky Dink® sheet and shrunk it down to make a mould. The ink lines printed on their Shrinky Dinks® were raised by over 500% to form a series of small walls with slightly rounded edges. With this method, the rounded channels with heights up to 80 um and width as thin as 65 um, have been consistently and easily achieved. The polydimethylsiloxane (PDMS) plastic that was used to make the devices could then be simply poured into the mould, cured, and peeled off. Using this approach the Berkeley team has fabricated a gradient generator and used these microchannels to flow mammalian cells. The figure shows the gradient generator filled with food dye. Professor Khine is reported to have said that researchers are excited about this, because it dramatically lowers the barrier to entry into the microfluidics field. There are no tooling costs, no clean room requirements, and the chips from design to device can be accomplished in a matter of minutes. By re-printing on the shrinky dink sheet, one can get walls of different thicknesses, which is not so easy with silicon moulds used for microfluidics. Professor Khine remembered her childhood toy material when she was faced with the problem of not having access to photolithography equipment to make microfluidics devices. Necessity, as they say, is the mother of invention.

Sources: http://pubs.acs.org/cen/news/85/i49/8549news2.html; Lab Chip, 2008, 8, 170 - 172, DOI: 10.1039/b711622e - Shrinky-Dink microfluidics: rapid generation of deep and rounded patterns; www.shrinkydinks.com.

Accomplishments: LTCC in C-MET, Pune

Girish Phatak

With the rate of miniaturization of devices in the Integrated Circuits tapering off, the focus has now shifted on improving the systems performance through developments in packaging. The buzz word today is of systems integration and miniaturization. Realizing this, Centre for Materials for Electronic Technology (C-MET), Pune, had initiated a programme in Electronic Packaging from the beginning of the 10th Plan, i.e., year 2002. The programme received a shot in the arm in 2004, when the National Programme on Smart Materials (NPSM) (see Vol. 1, p. 1) generously funded the establishment of a complete fabrication line for the Low Temperature Co-fired Ceramic (LTCC) process technology.

LTCC is a multilayer circuit fabrication process that offers immense advantages. It is characterized by high interconnection density, high frequency (HF) capability up to a few 10's of GHz, capability to integrate passives, capability to form open and buried cavities, compatibility with wire-bonding and flip chip processes, matching TCE with Si and GaAs, high working temperatures and high reliability.

Today, C-MET, Pune, possesses a 1500sq. ft Class 10,000 clean room that houses a state-of-the-art LTCC fabrication line, capable of prototyping and small-scale production. The facility also includes a photolithography set-up and package sealing equipment. The prominent equipment include: programmable via punching, screen and stencil printer, green-tape stacker, green-tape cutter, isostatic laminator, programmable batch furnace, belt furnace, solder reflow oven, seam sealer with glove box, mask aligner, and solder ball shear testing machine. The facility was commissioned in 2006 by Dr. V. K. Aatre, former Scientific Advisor to Raksha Mantri and Chairman, B-SMART.

A hermetically sealed package (top) with interconnections across the multilayer LTCC lid made at C-MET, Pune

The LTCC process line of C-MET has proven its capability of fabricating via up to 200µm and placing them in aligned or staggered configuration, conductor lines and space up to 200µm, multilayering capability up to 20 layers, fabrication of rectangular and round shaped open cavities, preparation of bond-shelves and wire-bonding pads, hermetic package sealing and Ball Grid Array (BGA) preparation. Some important contributions of the Group, in terms of process development, include the process of BGA formation by stencil printing, development of electroplating process for depositing solder films up to 300µm, development of process for preparing hermetically sealed packages with interconnections to a specially fabricated multilayer lid (see figure), and, capability to integrate buried heater and thermistor. The latter would be quite handy in developing devices in realm of miniature bio sensors.

The LTCC process offers great opportunities in integration of microsystems with electrical, mechanical, optical, microfluidic and gaseous interconnections across the package. The MCM and the 3D packaging capabilities of LTCC, coupled with microwave integration, offers good opportunity in miniaturizing various electronic systems. The layer-by-layer processing presents even more innovative possibilities, hitherto unreported. C-MET welcomes 'applications' partners in realizing these.

Dr. Girish Phatak is a scientist in C-MET, Pune. He can be reached at gjp@cmet.gov.in.

S Ū K S H M A
Institute of Smart Structures and Systems
Department of Aerospace Engineering
Indian Institute of Science
Bangalore - 560012
India