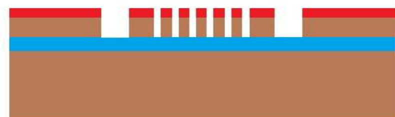
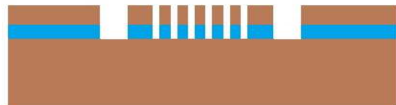
TYPICAL PROCESS FLOW

SOI wafer, Resistivity <0.005Ω-cm
Device layer: 30 μm
B-OX: 4 μm
Handle Layer: 400 μm

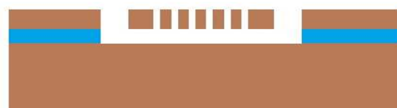
Mask 1: Photolithography ,
Minimum dimension >3um



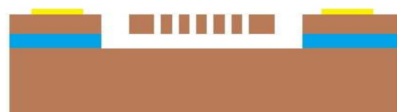
Etch: DRIE, Silicon 30μm



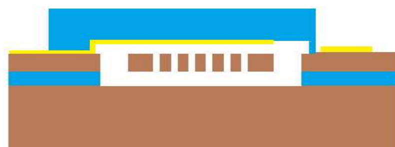
Etch: Dry Etch, Silicon di oxide



Release:Wet Etch Silicon di oxide



Metal Deposition:
Aluminumupto 1 μm,
Goldupto 0.5 μm



Capping by Anodic Bonding (Glass)
Glass cavity depth: 5μm
Electrode formation by Metal Deposition: Gold upto 0.5μm

<u>Design Rules</u>

1. Gap between combs: > 3µm
2. Comb/Beam width: > 3µm
3. Perforation size: >/= 8µm X 8µm
4. Distance between perforations: >/=12µm (on all sides)
5. Gap between proof mass and electrode(in capping wafer) : < / = 4.5µm
6. Device layer thickness of SOI wafer is 30µm, hence the structure has to be of 30 µm thickness.

Note: Participants are required to adhere to the design rules above, that are framed as per process requirements/constraints.