PMRF-ISSS Teaching Programme

Prime Minister Research Fellowship students' teaching requirement facilitated by the Institute of Smart Structures and Systems

Module PMRF-ISSS076

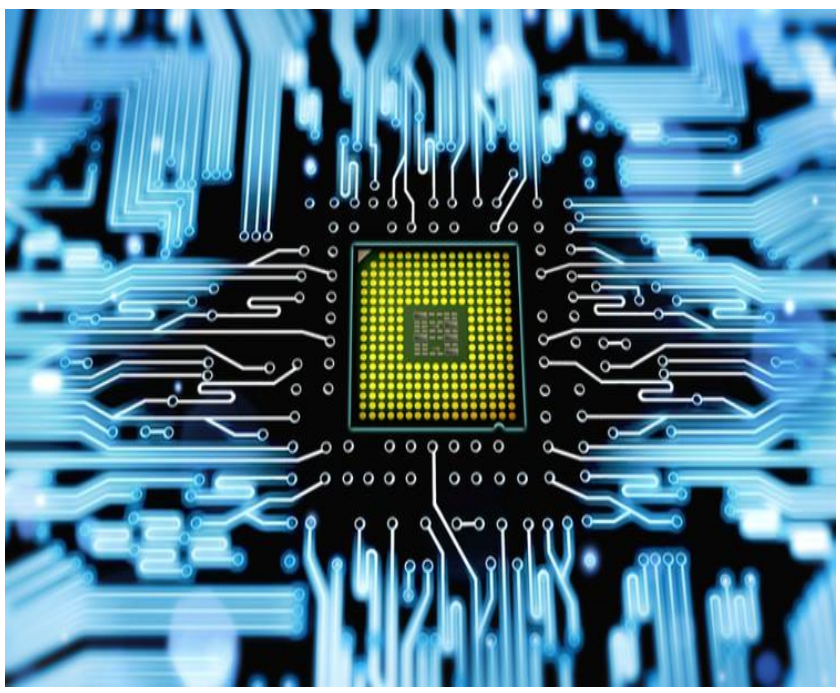
Digital Design with Verilog

Name of the PMRF student

Krishna Sai Tarun Ramapragada

Required background of the students taught

- UG Students of Electronics Engineering, Electrical Engineering



Details of the content of the module

Verilog:

1. **Basics of FPGA and ASIC**
2. **Behavioural Verilog with examples**
3. **More on blocking, Non-blocking statements and recommended practice**
4. **Dataflow Verilog with examples**
5. **Example design of up-down counter**
6. **Design of Finite State Machines**
7. **Example design of Simple ALU**
8. **Example design of non—pipelined and pipelined Booth Multiplier**

Static Timing Analysis:

1. **Set up and Hold time**
2. **Min and Max delay constraints**
3. **Example problems**

Exploring open-source tools:

Icarus Verilog, Yosys and Open STA

Schedule of the module

Start Date: May 21, 2024

End Date: August 09, 2024

Total Duration: 36 - 40 hours

Class Schedule: Every Tuesday and Friday

Class Timings: 7:00 pm to 8:30 pm IST (1.5 hour)

Meeting link : Will be shared later

Link

Contact email ID: isss.forum@gmail.com

Registration link:

https://forms.gle/xoFQvmc6YxJxmqgj9