PMRF-ISSS Teaching Programme

Prime Minister Research Fellowship students' teaching requirement facilitated by the Institute of Smart Structures and Systems

Module **PMRF-ISSS053/III/2025**

RISC-V Processor System Design

Name of the PMRF student

Krishna Sai Tarun Ramapragada

Required background of the students taught

- UG Students of Electronics Engineering, Electrical Engineering

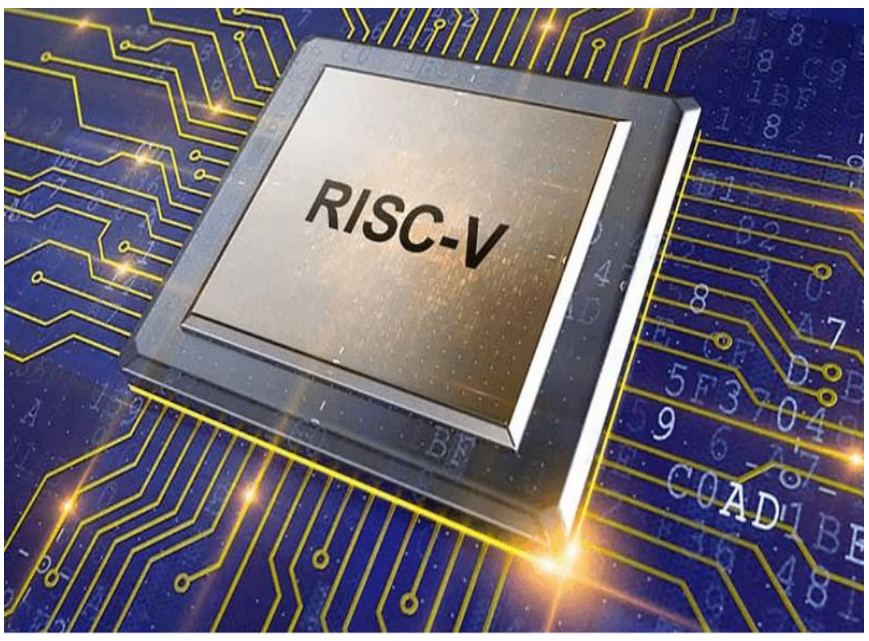

Image Source: https://www.dfrobot.com/blog-13481.html

Details of the content of the module

Module 1: (~ 6 hours)

- **RISC V Basics**
- **Overview of Single Cycle Processor Design**

Module 2: (~ 18 hours)

- **Pipelining**
- **Hazards in Pipelining**
- **RISC V Pipelined Processor Design (including design for hazard detection, forwarding and stall)**

Schedule of the module

Start Date: May 31, 2025

End Date: August 16, 2025

Total Duration: 24 hours

Class Schedule: Every Saturday

Class Timings: 11:00 am to 1:00 pm IST (2 hours)

Meeting link : Will be shared later

Link

Contact email ID: isss.forum@gmail.com

Registration link: https://forms.gle/b23f3fTAi19fbf9C8