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INSTITUTE OF SMART STRUCTURES AND SYSTEMS

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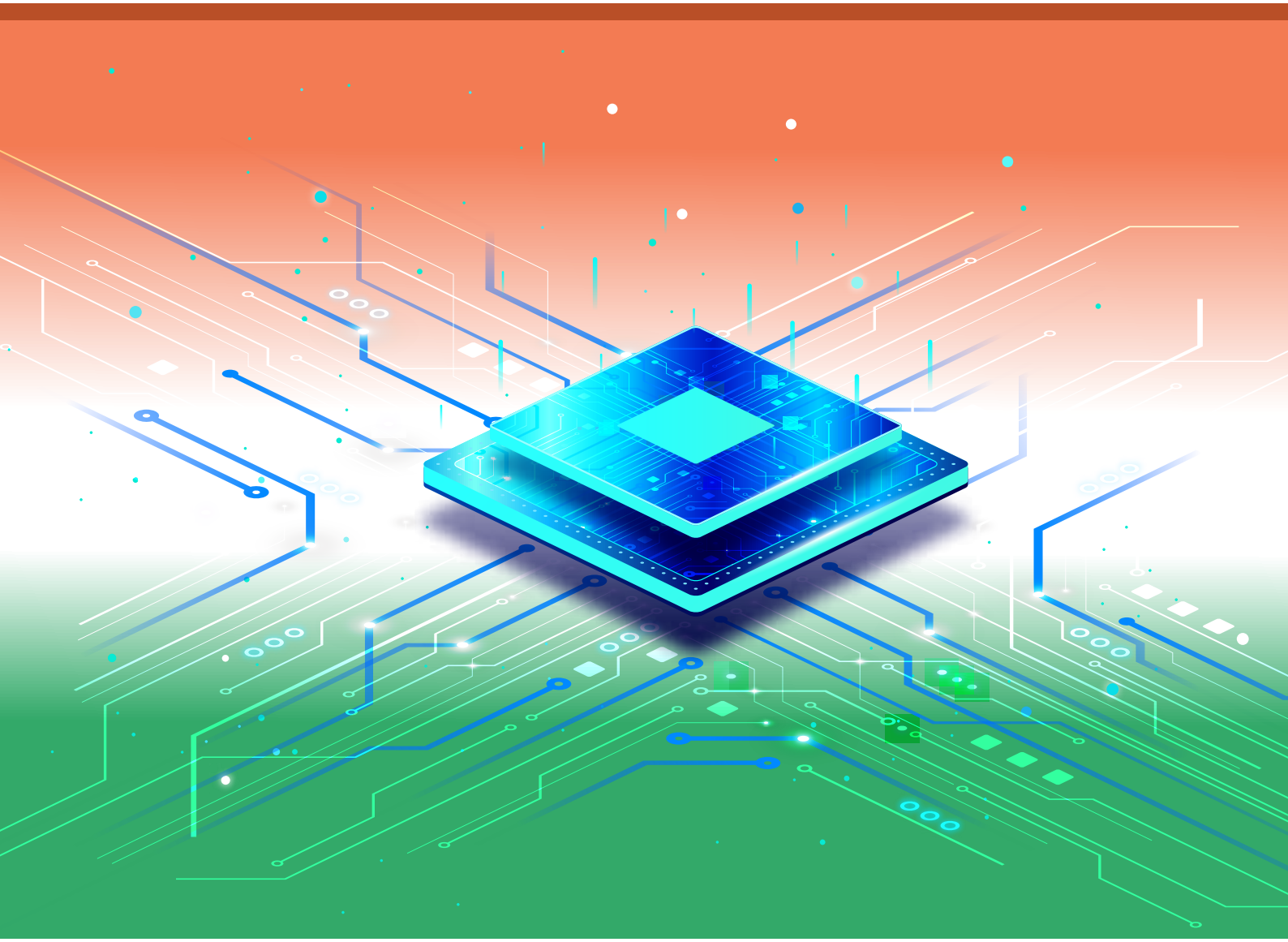
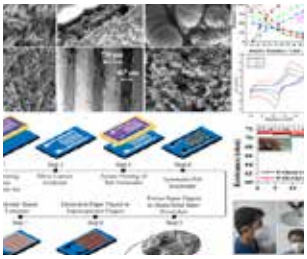


GLIMPSES OF THIS ISSUE

AWARDS

ARTICLES



BOOK REVIEW

CONTENTS

1 President's Message

DR. VIDYASHANKAR BURAVALLA

The new issue of revived Sukshma is in your hands! Thanks mainly to the newly formed Editorial Board, spearheaded by young and energetic Dr. Nilanjan Chattaraj! I am sanguine that Sukshma would again be regular, exciting and enriching your experience.

There are indeed lot of events and activities of ISSS in the recent past which we would like to bring to your attention. During and post Covid pandemic, ISSS continued to be active and organized several events and activities on-line. Especially, under the able leadership of Prof. Ananthasuresh, several new activities were initiated and are being run successfully. To name a few, PMRF Lectures, Sukshma Webinars and Lectures, Short-term courses in the areas of MEMS Design, Bio-Mems and ISSS community chip. In addition, recently SITAR and ISSS conducted a national student MEMS design contest as a part of 75th Year of Indian Independence. Notwithstanding the short notice, ISSS was able to publicize the event and mobilize the MEMS Community in Academia in the country to submit their entries. The success of this event has now led to plan to make this an annual event.
As you are all aware, ISSS has annual awards in different categories, ranging from UG student awards to Young Scientist and Technology awards. Last year we got a good number of nominations and that too pan India. This is a clear indication that lot of interesting and noteworthy work is going on across the country and in institutions other than the IITs and IISc. A very encouraging sign indeed!

Another initiative that promises exciting days ahead for ISSS is the tie-up with IEEE Sensors Council in India for the conduct of international conference on Sensors and Sensor Systems-APSCON-23. This is scheduled for January, 23-25, 2023 and to be held in Bengaluru. I urge ISSS community to make best use of this opportunity to both showcase their work and to learn about new developments in this rapidly developing technology domain. Thanks to the sustained efforts of Dr. Veda, ISSS has constituted four sub-committees, each looking into a strategic area to enhance the impact of ISSS. While some of you are already either participating in these activities or aware of these, we would be covering a more detailed write-up on these in subsequent editions of Sukshma.

I am sure all these developments herald a new and exciting phase for ISSS! Hence, I request you all to make ISSS even more impactful by active participation in all its events and activities and more so by bringing in more and more members into the ISSS fold.

2 ISSS PMRF Lecture Series

ISSS is providing an online teaching platform to Prime Minister Research Fellows (PMRFs). These are being attened by engineering and other streams of undergraduate and post-graduate students. PMRF is a programme of the Government of India, details of which can be found at https://dec2020.pmrf.in/. Under this programme, selected PhD scholars at IISc, IITs, and IISERs are recognized with the PMRF based on their academic and research performance. There is a requirement that PMRFs should also teach outside their institution for at least one hour per week, on the average. Under this activity, 17 courses were offered by PMRFs in IISc during the year 2021. Many PMRFs have compelted their teaching. Details of the enrollement and course titles are furnished here

S. No.	Course title	Enrollment
1	Analog Electronic Circuits	292
2	Introduction to Deep Learning with Python	496
3	Molecular Biology	1172
4	Mechanics of Beams	24
5	Semiconductor theory	46
6	Digital Signal processing	24
7	Compliant Mechanisms	51
8	Cell Biology	992
9	Cell Mechanics	759
10	Introduction to Random Processes using Python	110
11	Basics of Ansys Fluent	122
12	Printing Technology	177
13	Micro-Nano Fabrication and Characterization	142
14	Continuum Mechanics	310
15	Finite Element Analysis	320
16	CRISPR	2655
17	Fluid Dynamics	10

The recordings of the lectures have been made available on the ISSS portal for the particpants to view. These courses are continuting futher in 2022 and the full list of courses and flyer can be found on ISSS website link https://isssonline.in/pmrf-student-lecture-series/

Some testimonials from PMRF students and participants are included.

Harshal Srivastava

"I am Harshal Srivastava, M. Sc., currently focused on molecular plant virology, and I joined the course with the expectation of a general cell biology extension. However, more than that, It was fully convincing with the course flow, excellent course content, delivery method, and one-to-one interaction on the first-class, later also problem-solving sessions.

In the course, I abide by how cells can sense, respond and exert mechanical forces under a specific environment. Their mechanical properties and correlation with cellular function and its quantification techniques. The end of the course gave me a broadened perspective of looking at a biological system, and hopefully, I shall use the cell mechanics concept in my research journey."

"As a PMRF fellow, I taught Digital Signal Processing online to students. The experience has greatly helped me in improving the way I communicate technical ideas. As the students had a diverse background, I had to teach from first principles, and this evolved my understanding of the subject. The overall platform provided by the ISSS was hassle-free, and I could focus on the teaching material, rather than administrative tasks. I would hope that ISSS continues to provide this support to students."

Manu Gulyani

Neethu S. Nithyananda

"Firstly, I would like to thank ISSS and IISc Bangalore for providing an excellent online course in this COVID pandemic. This course is helping to build the basics of micro-nano fabrication and characterization. The course is introduced from basics, so it is easy to understand concepts clearly. Every slide is so informative and easy to understand. Communication language is easy to understand. Recalling the concept from previous lectures helps us to connect to the following concepts. Summarising concepts at the end of the lecture helps in memorizing and clears concepts profoundly. Recorded lectures help to clear doubts and stay in touch with the course if we miss any lecture. Thank you for giving us the opportunity to attend this course. I kindly request to provide more and more courses which help us to get into the research field."

"I am indebted to ISSS for giving me the fantastic opportunity to teach a course on 'Cell Mechanics'. Not only did they provide me all the necessary tools and an online platform to teach the course, but I also received a lot of help from the course coordinators. While I got the chance to teach my favourite subject, it also served as a good learning experience for me."

Anwesha Barua

3

A Brief Report on ISSS Awards 2021

The ISSS endeavors to motivate young students and young researchers by providing them recognition for their research contribution under five categories through ISSS-awards. Last year ISSS has received a commendable number of participants for its award scheme. Under UG category we received 11 nominations, under PG category we received 4 nominations, under Ph.D. category we received 16 nominations, under Young Scientist award category we received 6 nominations and under Technology Award category we received 3 nominations. There were two distinct committees to evaluate the nominations and select the award winners. ISSS whole-heartedly appreciates the effort and time given by the committee members to select the winners. Prof. Ashok Kumar Pandey of IIT Hyderabad, Prof. Siva Vanjari of IIT Hyderabad, Prof. Gangadharan of NITK Suratkal and Prof. Mira Mitra of IIT Kharagpur were in the evaluation committee for the student-award category. Prof. Ashok Kumar Pandey of IIT Hyderabad was the chairperson for this committee. Whereas Prof. Shashikala Gangal of University of Pune, Prof. M. M. Nayak of Indian Institute of Science and Dr. Chandrashekar of BigTech were in the evaluation committee for the Young Scientist and Technology Awards category. Prof. Shashikala Gangal was the chairperson for this committee. The ISSS Awards 2021 online ceremony was held on 26th March 2023. Here are some of the moments captured during the online ceremony of ISSS Awards 2021. The details of award winners under various categories are listed below. The same information is also available in the website of ISSS: https://isssonline.in/isss-awards-2021/

Category	Winner	1st Runner Up	2nd Runner Up
UG	Mr. Achintya Dutta, Manipal Institute of Technology, Manipal	Mr. B. Hemanth, Ms.Chethana M, Mr. Kishore NMIT, Bangalore	Mr. Rahul Kamath, Mr. Rakshith P, Mr. Rohan Sathish, BMSCE, Bangalore
PG	Mr. Shubham Bhatt, Rustamji Institute of Technology, Gwalior	Ms. Diksha Singh, CERRI Pilani, Pilani	Mr. Ajay Kumar Sahu, Manipal Institute of Technology, Manipal
PhD	Dr.Murugappan Ranganathan, IISc, Bangalore	Dr.Sanghamitra Ghosh, IIEST Shibpur	Dr.Priyank Mukeshkumar Shah, IIT Delhi, Delhi

Category	Winner	Institute / Organisation	
Young Scientist Award	Dr. Koushik Guha	National Institute of Technology Silchar	Joint winners
	Dr. I. A. Palani	Indian Institute of Technology, Indore	
Technology	Team award	IIT Madras Research Park	

In this issue of Sukshma we have included articles contributed by the awardees under UG and PG categories. The articles contributed by the awardees under the PhD, Young scientist and Technology award category will be included in the coming issues of Sukshma.

UG WINNER

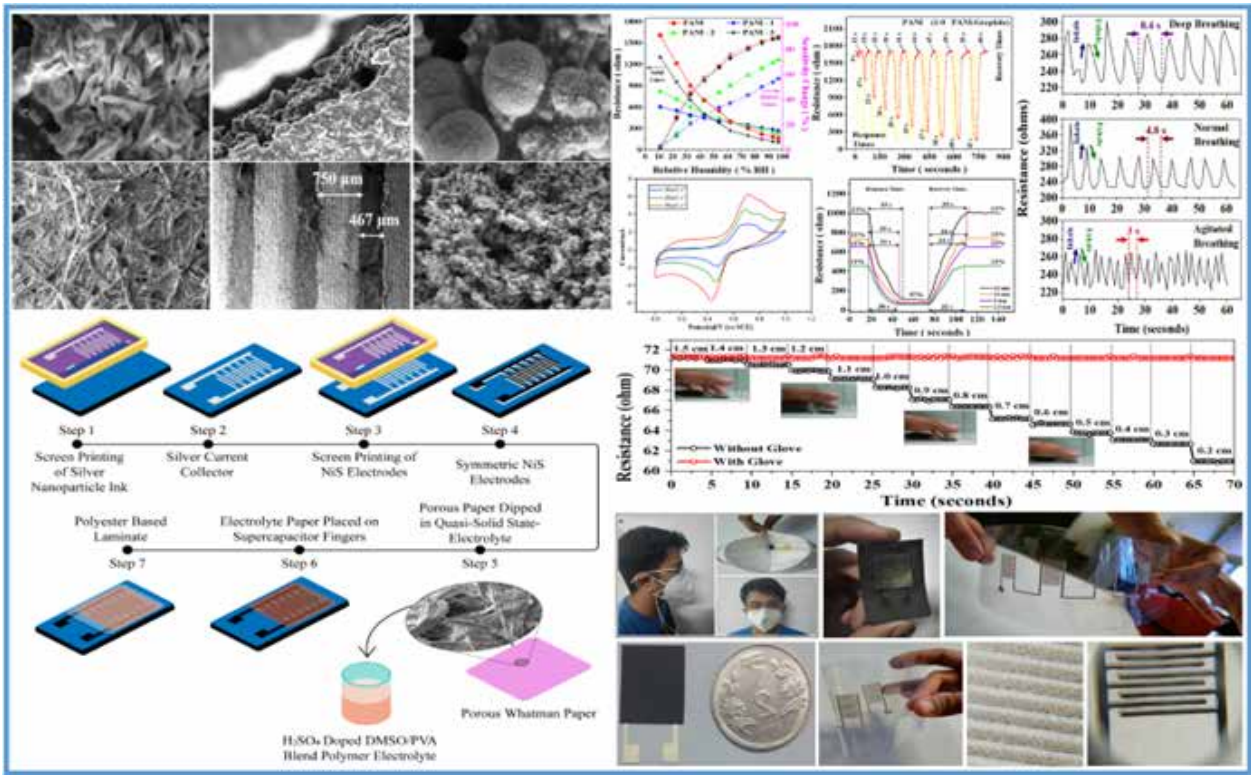
Sensitivity tuned pani/graphite nanoparticle based humidity sensor powered by cu/graphite micro-supercapacitor with pva/pvp polymer electrolyte

Achintya Dutta,
Manipal Institute of Technology

ISSS Awards 2021 - UG: Winner

Out of all the families of materials which have been explored for humidity sensing such as transition metal dichalcogenides and metal oxides, conducting polymers have shown the most promising results. Polyaniline is one such conducting polymer that has shown immense potential due to its high stability, low cost, simple methods of synthesis and high hydrophillicity. But due to its positive temperature coefficient, mainly attributed to the phonon emissions occurring during the tunnelling of electrons in the polymer chains, there exists an interdependency between temperature and humidity. Thus, to overcome this challenge, we demonstrated that the addition of graphite as the support material to H_2SO_4 doped polyaniline chains not only improved sensor parameters such as response/recovery times (30s/32s), hysteresis (1.01%) and sensitivity (98%), but also resulted in higher thermal stability which eliminated the interdependency between temperature and humidity. This polyaniline/graphite nanocomposite was screen printed on a flexible PET substrate with Ag nanoparticle based current collectors to achieve a two dimensional flexible device on a 2.6 cm^2 surface area. We further integrated the fabricated humidity sensor inside an N95 mask and demonstrated that the sensor could accurately map the breathing patterns of a human test subject in real time due to the change in relative humidity inside the mask during inhalation and exhalation. Another major novelty introduced by us was the integration of a printed micro supercapacitor with the humidity sensor on the same flexible substrate, to serve as a power source and eliminate the requirement of a battery. A Cu/graphite based micro supercapacitor was screen printed on the same PET substrate, and a novel methodology was devised to deposit the electrolyte. A porous fibrous structure was used as the medium to deposit the PVA/PVP based quasi-solid polymer electrolyte, which overcame several disadvantages of conventional electrolyte deposition methods such as drop casting. All of this work resulted in two journal publications, one of which is currently under review, and a patent filed in December, 2021. As an extension of this work, we are currently working on the synthesis of two dimensional materials such as MXenes by etching and delaminating their MAX phase to study their interaction with water molecules to

further develop sensors with higher sensitivity and faster response times. This work is further being supported by carrying out DFT simulations to study the role of nearly free electron (NFE) states on the adsorption of water molecules on the surface of these two dimensional materials.



UG 1st RUNNER- UP

Simulation and Fabrication of Tungsten Oxide Thin Films for Electrochromic Applications

Mr.B.Hemanth,
Ms.Chethana M,
Mr.Kishore, NMIT, Bangalore

ISSS Awards 2021 - UG: 1st Runner Up

The main objective of the project is to improve the colouration efficiency and obtain a faster colour response. In order to improve the response time, the electrochromic device is modelled and simulated. The device is then fabricated and its properties are characterised using Electro-chemical Analyser and UV Visible Spectrometer. For simulation, planar and nano- pillar structures are modelled. The planar structure consists of a block of the electrochromic material. For the nanopillar structure, the block of electrochromic material is divided into smaller columns. This increases the surface-to-volume ratio of the nano-pillar structure. Due to higher surface-to volume

ratio, more ions are intercalated in the material. This increases the reduction and oxidation currents in the device. The modelled structure is fabricated by deposition using a DC Magnetron Sputtering method. The electrochromic material tungsten oxide is deposited on the substrate FTO glass as a thin film. For nano-pillar deposition, Glancing Angle Deposition (GLAD) technique is used.

The structural and material properties were analysed using Scanning Electron Microscope and X- Ray Diffraction. The electrical and optical properties of the deposited thin film is characterised using Electro-chemical Analyser and UV- Visible Spectrometer. The results from Electro-chemical Analyser show that the reduction and oxidation peak currents in nano-pillar structure is higher compared to that of the planar structure. This leads to an efficient and faster coloration response of the electrochromic device. The optical transmittance of the device is measured using the UV-Visible Spectrometer. The nano-pillared structure exhibited lower values of transmittance compared to the planar structure, that is, it transmitted lesser amount of light. Hence, by comparison, the nano-pillared electro- chromic structure is best suited to develop an electrochromic device which will give efficient coloration response in less amount of time.

PG WINNER

Design, Optimization and Performance Analysis of Stable, Efficient and Eco-Friendly Perovskite Solar Cell

Mr. Shubham Bhatt, Dr. Chetan Pathak, Rustamji Institute of Technology, Gwalior

ISSS Awards 2021 - PG: Winner

From nearly 4 decades, polycrystalline solar cells are in service to the mankind. Instead, it does not reach to the last man in the line. It is still costly and hence not accessible by everyone. Perovskite solar cells (PSC) are the third generation of solar cells. They are flexible, low cost due to the simple fabrication and processing yet they are as efficient as the silicon solar cells. However, the major hurdles toward their commercialization are the lead toxicity and their stability as the widely used material methylammonium lead iodide ($MAPbI_3$) is prone to degradation when comes in contact with humidity or water. To make it eco-friendly, the non-lead counterparts are need to explore [1,2]. Tin (Sn) based and Germanium (Ge) based perovskites are the most potential candidate for future generation of PSC. Where Sn-based PSC are quite explored, Ge-based is not. Hence, we at Rustamji Institute of Technology, Gwalior in collaboration with Prof. S K Pandey's Sensors and Optoelectronic Research Group (IIT Patna) explored the Ge-based PSC in our works and presented a theoretical framework for modelling the lead-free PSC.

In one of our works [3], we explore the methylammonium germanium iodide (MAGeI3) in a planar p-i-n architecture (Fig.1) consisting of indium tin oxide (ITO)/poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS)/$MAGeI_3$/ phenyl-C61- butyric acid methyl (PCBM)/Au. With this, we tried to understand its performance limiting factors. Our study was focused on the effect of various defect-related parameters on the performance of the cell. For this, the defect distribution is modelled and recombination models are applied. The TCAD simulations have shown the performance is greatly affected by the various defect parameters like defect density of states (DDOS), the FWHM of the deep-level DDOS, capture cross-section area of the defect and the interface defect density. We found that if

DDOS in the band tails if reaches 10^{18} cm^{-3} eV^{-1} or greater, then the performance degrades drastically which is due to increased SRH recombination. Characteristic decay energy or width of band tails which is related to the degree of disorder in crystal and also represents the penetration depth of band-tails into the forbidden gap is varied next. Characteristic decay energy up-to 40meV shows no significant reduction in power conversion efficiency (PCE) and after that efficiency decays linearly because their impact on carrier mobility becomes more prominent as it is now easier to trap the photogenerated charges. In the mid-gap, the DDOS when varied from 10^{16} to 5×10^{19} cm^{-3} eV^{-1} result shows rapid decrement in PCE because of trapping zone in the middle of the bandgap is now acting as a barrier to charge carriers. FWHM of mid-gap states represents the spread of defects or trap levels. PCE degrades rapidly as FWHM increases above 100 meV. Considering the effect of capture cross section of defect, with its rise the probability of capturing the charge increases and hence PCE degrades. The thickness of $MAGeI_3$ is varied and the optimized thickness is found to be 800nm. The effect of interface defect density is also studied which tells it should be under 10^{15} cm^{-2}. Hence, by optimizing the device parameters, we have achieved a simulated conversion efficiency of 13.35%. We hence tried to optimize these defect-related parameters for the best performance.

In another work [4], we explored the non-planar architecture as shown in Fig.2, consisting of ITO/ ZnO Nanorod(NR)/$CsGe_{0.5}Sn_{0.5}I_3$/Spiro-OMeTAD/ Au. Because of several advantages over planer structures like radial charge separation, better light trapping, and larger surface area to volume ratio. Attempts have been made earlier resulting in lower performances hence a detailed analysis for understanding the problem is necessary. To simulate such a complex mesoporous structure successfully, an identical section of this cell is simulated in 3D TCAD software. The model is then

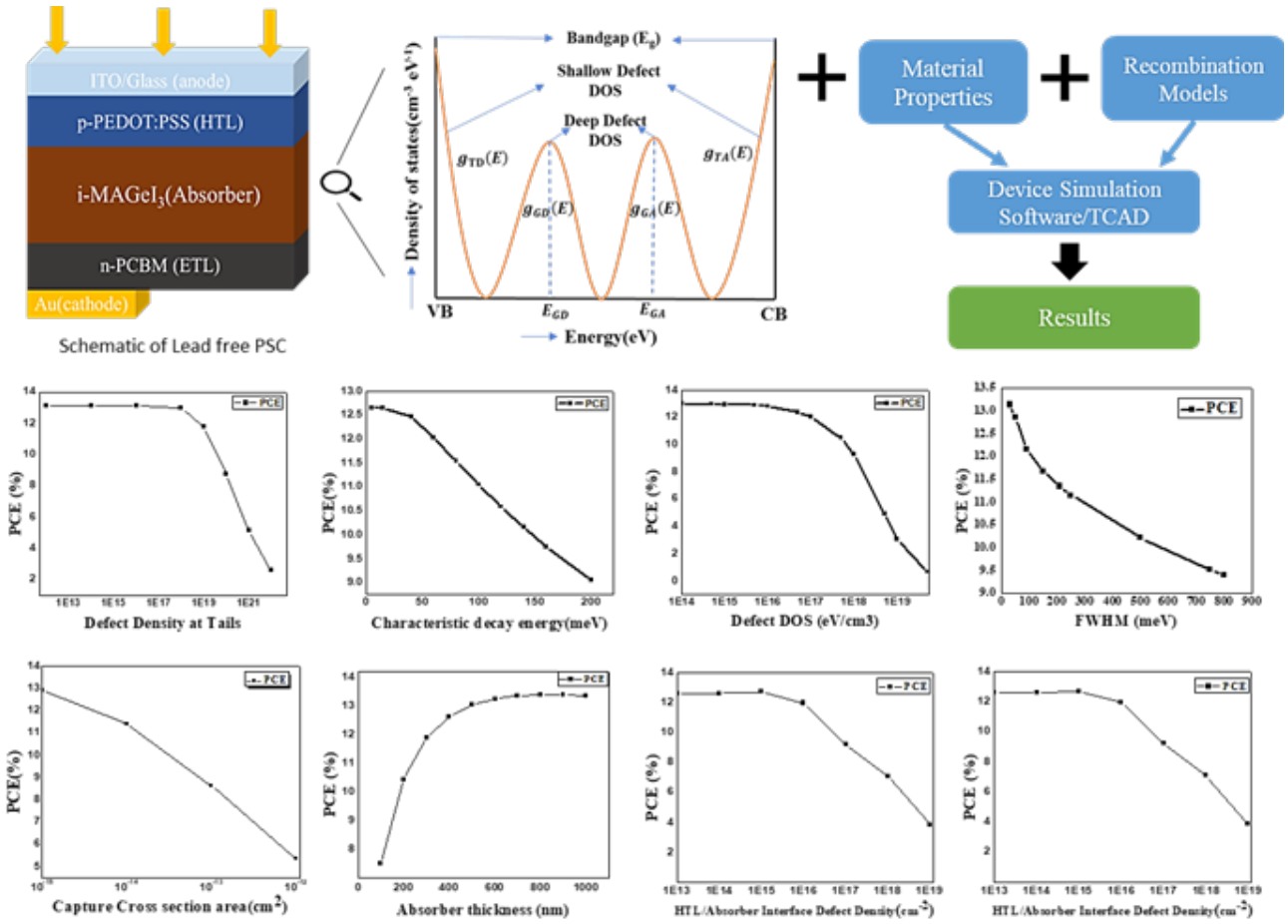


Figure 1: Detailed Analysis of effect of various defect related parameters in a MAGeI3 based PSC

well validated with various available experimental studies in the literature. Structural optimization is necessary in order to get high performance. Here we did an investigation of the effect of length, diameter and tilt of ZnO NRs, the thickness of the perovskite shell, thickness of the hole transport layer (HTL) cap, the effect of bulk and interface defect density on the performance of the cell. The optimized length and diameter are found to be 400 nm and 40 nm respectively. The optimized thickness of the perovskite shell, perovskite cap, and HTL cap was found to be 60 nm, 200 nm, and 50 nm respectively. It is found that the performance is unaffected if the deep level DDOS and defect DOS at shallow level band-tails in the perovskite absorber layer are kept under $5x10^{14}$ $cm^{-3}eV^{-1}$ and $5x10^{17}$ $cm^{-3}eV^{-1}$ respectively. The interface defect density of HTL/Perovskite and ETL/Perovskite interface should be kept below $1x10^{10}$ cm^{-2} for high efficiency. Performance is superior when the tilt is 10-degree with respect to the incident light for a given intensity of light.

To conclude, in our works we have explored various design strategies and did a detailed analysis to understand the bottleneck in the performance of these lead-free PSC. Thus, we expect that these results will aid the researcher to choose suitable eco-friendly alternative materials for future perovskite solar cell.

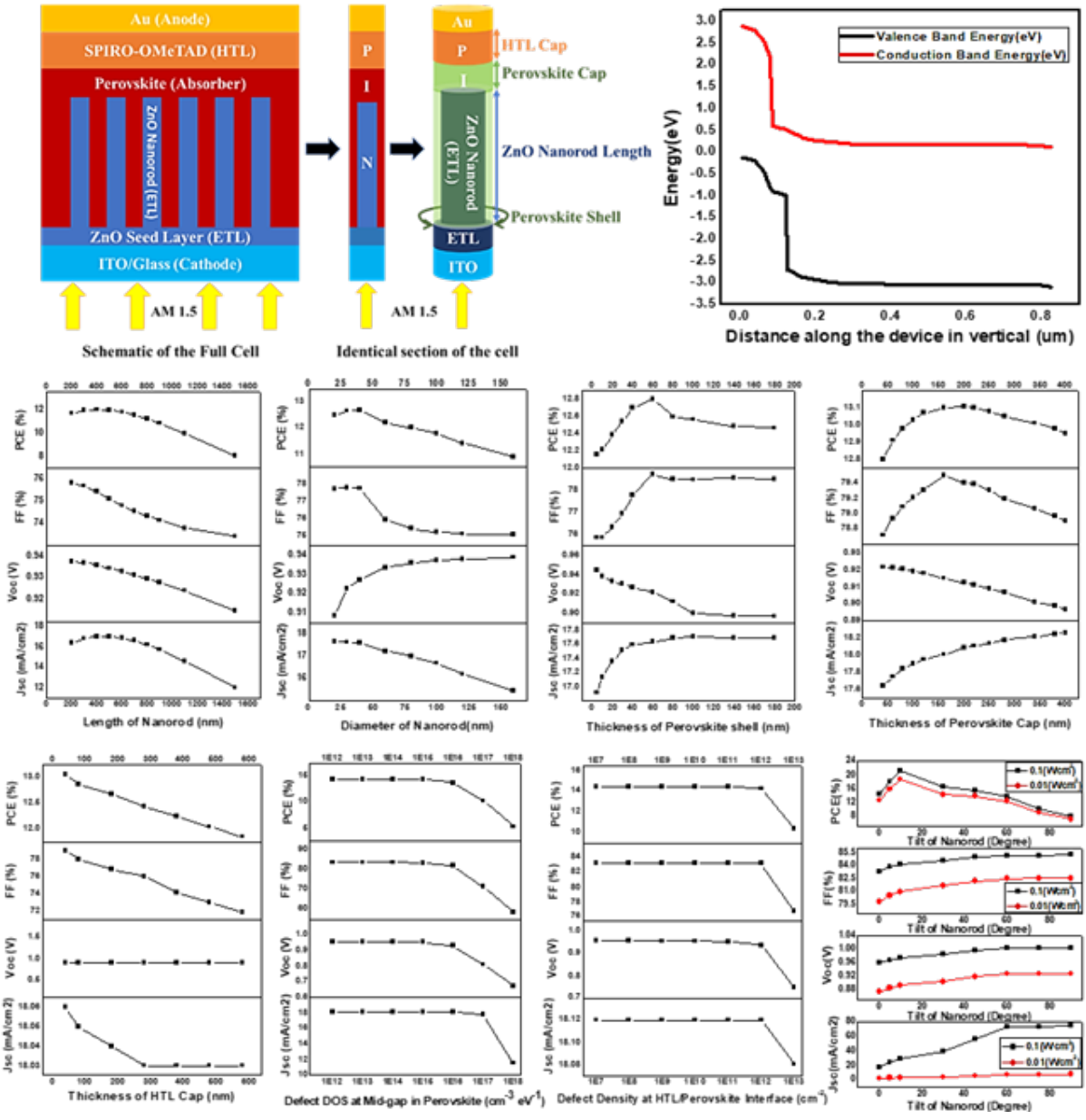


Figure 2: Structural optimization and Performance evaluation of a non-planar mesoporous lead free PSC

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PG 1st RUNNER-UP

Hardware Implementation of Posit Arithmetic and its FPGA Prototyping

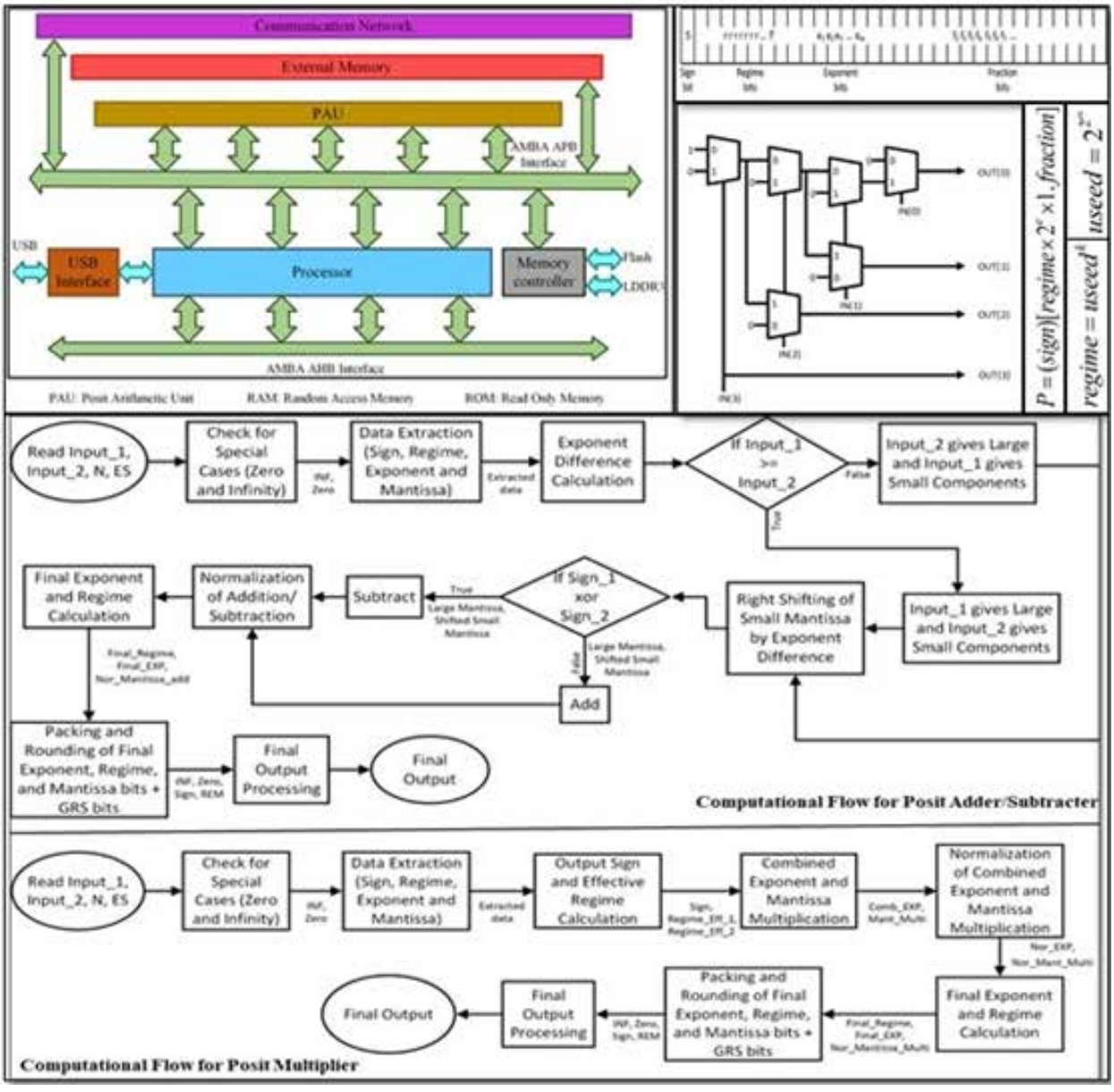
Ms.Diksha Shekhawat,
CEERI, Pilani

ISSS Awards 2021 - PG: 1st Runner Up

Modern electronic devices have embedded intelligence that allows for faster calculation and communication. High throughput, high data rate, fast computation, and low resources are necessary requirements for these engines. Here, fixed-point arithmetic can be suited for hardware implementations due to its simplicity of integer-based arithmetic. However, they are not able to be used in high-precision arithmetic. Here, floating-point arithmetic is well suited due to its extensive dynamic range. Although, hardware resources and power consumption are the limiting factors of floating-point arithmetic. Thus, there is a need for arithmetic that can provide accuracy closer to the floating-point and simplicity of operations like fixed-point arithmetic—a potential replacement for the IEEE-754 floating-point number known as posit proposed in 2017. A posit is a universal number (unum) that does not require interval arithmetic or variable size operands, and, like floats, it rounds off if the answer is not accurate. The amount of IEEE-754 research performed since its outset in the 1980s is nearly incalculable, and it has resulted in the optimized IEEE-754. Whereas posits are a manifestation of the Type-II unums numbers. There have been numerous software and hardware implementations of posits since the emergence of posit arithmetic. Posit just has one zero and one infinity. Furthermore, it ignores the subnormal or denormal representation, implying that all values are normalized. It adds additional bits to the mantissa for tiny real numbers and less bits for large real numbers, all within a fixed-length format. In contrast to float, posit provides many compelling advantages that include a more extensive dynamic range, higher accuracy, bit-wise identical results across systems, better closure, simpler hardware, and simpler exception handling. Apart from these, posit never underflow to zero or overflow to infinity, and not-a-number (NaN) indicates an action instead of a bit pattern. Posit consists of four components: sign, regime, exponent, and mantissa. The exponent size of an N-bit posit is used to interpret it. The sign bit is either

'0' or '1', indicating whether the number is positive or negative. In addition to the floating-point field, posit has a field called regime. The regime length is flexible and denotes the series of identical bits following the sign bit and ending with the opposite bit. The length of this sequence of identical bits is represented by k, which is positive when the bit is a '1' and negative when it is a '0'. Two numbers equal in posit addition by comparing their regimes and exponents and shifting them by the amount of bit difference. Once the regime and exponents are equal, addition can be performed on the mantissa bits. Overflow occurs if the mantissa is greater than or equal to '2', and underflow occurs if the fraction is less than '1'. The exponents do not need to be compared in posit multiplication, and there is no need for fraction alignment. The fraction bits are multiplied and added together to form exponents.

The key contributions of our work include an algorithmic flow for the posit adder/subtractor, multipliers, and their architectural design and implementations. They operate on N-bit input operands, ES-bit exponent size, an N-bit output. Observable methods for area and delay calculations have been used that provide a comparison of posit arithmetic with varied N and ES values. Observable methods for area and delay calculations have been used that provide a comparison of posit arithmetic with varied N and ES values. FPGA implementations are done on the Xilinx Virtex-7 xc7vx330t-3ffg1157 device. In the proposed work, LUT utilization is 7.11/16.07% lesser for 16/32-bit posit adders with ES=2, and 1.8% lesser for the 32-bit posit multiplier with ES=3, in comparison to the existing architecture.



PG 2nd RUNNER-UP

ASIC RTL Design Of MAC Engine For 2D Image Convolution

Mr. Ajay Kumar Sahu, Manipal Institute of Technology, Manipal

ISSS Awards 2021 - PG: 2nd Runner Up

The aim of the project was to come up with a standalone architecture that can perform 2D convolution on floating-point image data. The proposed MAC Engine uses two microcode processors (mcps) as controllers. These mcps are based on a small instruction set that is sufficient to implement for-loop-like algorithms. With these controllers, the convolution and related algorithm are implemented at the HW level as a part of this architecture itself thereby reducing the dependency on the host system. One of these controllers implements an image partitioning algorithm that partitions the image and distributes the image block data among the respective functional units. With this microcode processor, the MAC engine is able to achieve parallelism and it reduces the workload of the computationally intensive convolution process of the image. The other controller implements a sliding window algorithm for convolution. It performs linear indexing of pixel data & kernel weights and then sends it to the single-precision floating-point MAC units. We have proposed a modified version of this algorithm that takes care of the boundary conditions in the image window without any extra memory requirements for padding. Along with these algorithms, we have also proposed two modified arithmetic elements in the functional unit that are efficient compared to the conventional arithmetic elements. A low power multiplier based on dynamic range detection of pixels was found to be consuming less power without affecting the accuracy of multiplication results. An increment-by-one adder based on AND-XOR structure performs increment-by-one faster than a conventional adder. As the outcome of this work, we found that the resultant image has better PSNR compared to the same image obtained from MATLAB processing. The designed RTL was synthesized with gpdk-90nm technology library using the Cadence Genus tool.

I carried out this work under guidance of Prof G S Nayak and Prof Vishnumurthy Kedalya K at Manipal Institute of Technology, Manipal. This work has been published in IEEE Access which can be located at https://ieeexplore.ieee.org/abstract/document/9557274

5 India's Semiconductor Mission: Current Affairs

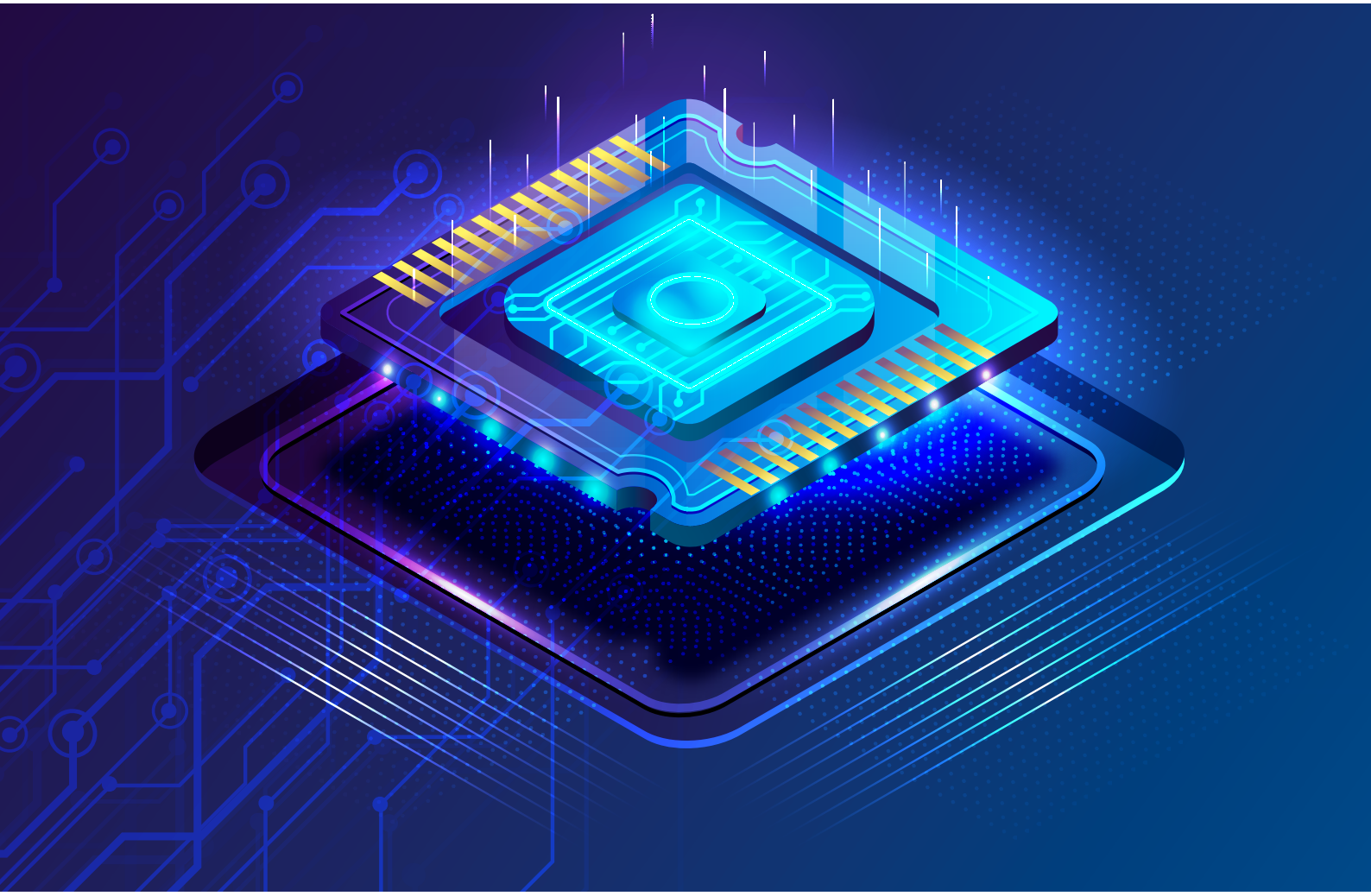
A nation's development is gauged by its ability to contribute towards sustainable development, for improving the lives of its own people while contributing to making the world a better place to live. United Nations adopted the Sustainable Development Goals (SDG) in 2015 with the aim of making the planet free of poverty, strife and to ensure that, by 2030, people globally enjoy peace and prosperity. Technology is one of the strong pillars for achieving the SDGs laid down by UN. Any nation which is able to create an infrastructure for innovation and creation of technology will forge ahead in providing sustainable development.

Semiconductor Technology is ruling the roost on technology front as it has influenced all walks of life. From driverless cars to spacecraft, from submarines to missiles, from e-rickshaw to bullet-trains, it is present everywhere. India at present is not self-dependent as far as chip manufacturing is concerned. Two years of pandemic has taught an important lesson of the need to be self-reliant in technology, specifically semiconductor technology. Self-reliance in semiconductor chip manufacturing will help India in manifold ways. Not only will it generate employment, but it will also establish a semiconductor manufacturing eco-system. The vision of an Atmanirbhar Bharat Abhiyaan in electronics and semiconductors has now led to the setup of India's Semiconductor Mission (ISM) as an Independent Business Division within the Digital India Corporation (https://dic.gov.in/index.php/divisions/india-semiconductor-mission). The mission aims at establishing the semiconductors and display manufacturing facilities along with the semiconductor design ecosystem. Under this mission, Semicon India programme with a total outlay of INR 76,000 crore for the development of semiconductor and display manufacturing ecosystem was announced on 15th Dec 2021 and FOUR Schemes were announced on 23rd March, 2022 (https://pib.gov.in/PressReleasePage.aspx?PRID=1808676) viz., (i) setting up of semiconductor fabs (ii) setting up of display fabs (iii) setting up of Compound Semiconductors / Silicon Photonics / Sensors Fab and Semiconductor Assembly, Testing, Marking and Packaging (ATMP) / OSAT facilities in India (iv) Design Linked Incentive Scheme (DLI)

Academia and R&D organizations are going to play a big role in the DLI scheme by providing trained manpower for development and deployment of semiconductor design for Integrated Circuits (ICs), Chipsets, System on Chips (SoCs), Systems & IP Cores and semiconductor linked design.

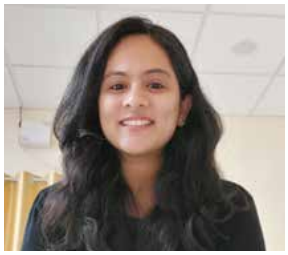
Readers are requested to watch out for this space for more information of this topic.

6 सूक्ष्म संरचना Sukshma Samrachana: 21 MEMS Innovation Challenge Highlights



The Sukshma Samrachana 21 event was organized by Semiconductor Technology & Applied Research Centre (STARC) in association with ISSS. The contest was launched on 15th September 2021. We received around twenty four contestants from several reputed institutions such as, Indian Institute of Science, Indian Institute of Technology Delhi, Indian Institute of Technology Mandi, University of Calcutta, Institute of Radio physics and Electronics, Birla Institute of Technology and Science, Pilani, Saveetha Engineering College, Annamalai University, Nitte Meenakshi Institute of Technology, Nitte Meenakshi Institute of Technology, AIET,Moodbidre, Raja Lakshmi Engineering College, Alva's Institute of Engineering and Technology. There were two stages of evaluation. The ISSS acknowledges the Engineers, Scientists and Professors affiliated with DRDO, NAL, ISRO, Tyndall National Institute Ireland, Indian Institute of Science Bangalore, General Electric and Indian Institute of Technology Madras for being part of the evaluation committee. The final evaluation concluded the following winners for the Sukshma Samrachana 21 MEMS Innovation Challenge.

Winners of
MEMS Innovation Challenge

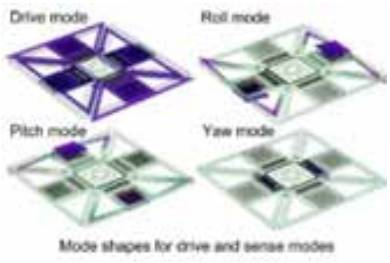


FIRST PRIZE

Ms. Pradnya Chabbi, BITS, Pilani

PAPER TITLE

Design and analysis of inertial grade wide range single drive three axis MEMS gyroscope



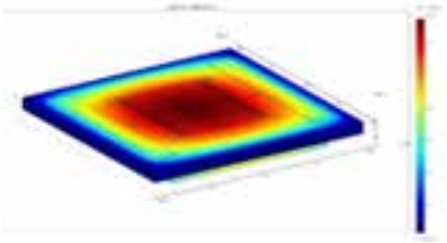
Simulation results of the gyroscope

SECOND PRIZE

Mr. Shirshendu Chateerjee, Institute of Radio physics and Electronics, Kolkata

PAPER TITLE

Design of MEMS Based Mini-Catamaran



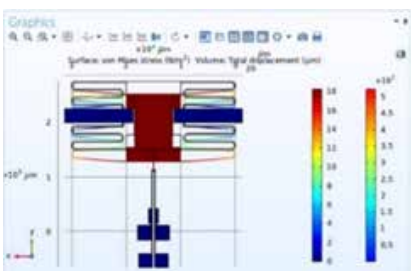
Simulation results of the micro heater

THIRD PRIZE

Mrs. R. Kavitha, Mr. P. Madhan Kumar,
Mr. Suriya Kumar, Mr. Vimalraj
Raja Lakshmi Engineering College, Chennai

PAPER TITLE

Single axis G-switch for high-g application



Simulation results of the G-Switch

Position	Prize amount
First	Rupees One Lakh
Second	Rupees Seventy Five Thousand
Third	Rupees Fifty Thousand

The awards Ceremony was conducted at STARC, Bangalore on 17th December, 2021 during Azadi Ka Amrit Mahotsav Celebration and STARC Product Launch. The awards were presented by Dr. K.S. Varaprasad, DG, HR, DRDO.

7

Book Review

Book Review: PRIMER on ENGINEERING STANDARDS by Maan H. Jawad and Owen R. Greulich ASME Press, 2014

Prof. G. K. Ananthasuresh, IISc Bangalore

It is well known that standardization helps in any activity to ensure functionality, safety, quality, repair, maintenance, and interoperability. It is difficult to imagine a world without standards. It is not an overstatement if we say that they have been in existence, in some form or other, ever since human civilization started. Industrial revolution made it imperative to establish standards so that products and processes are widely shared across countries and continents. Despite the significance of standards in our daily life, it is a subject that it rarely taught in a university and is also rarely pursued as a research activity. Standardization is often the task of governments, the industry, and professional societies. That is probably why we have a book "Primer on Engineering Standards" published by the American Society of Mechanical Engineers (ASME). This book focuses on engineering standards as its title clearly states.

The brief about the book conveys the purpose of engineering standards succinctly: "…They (the standards) supplement the design process by guiding the designer or user to ensure consistent products with safe and reliable operation. Understanding and complying with pertinent standards helps to ensure a successful design, fabrication, and operation of a product." From this, it becomes clear that this book has a tilt towards gaining an understanding of the standards from the viewpoint of design. So, the book is written from the perspective of people who want to design a product. Therefore, it does not give an elaborate account of the history of standards or how standards came about. Rather, it starts off by stating what engineering standards entail. They include rules, codes, regulations, and jurisdictional requirements. Thus, with the very first sentence of the first chapter, the authors mean business: they want to educate the reader with precise information rather than rambling about standards. They go on defining each of the forementioned terms that entail engineering standards. By giving the classification of standards (as "limited consensus general consensus, and governmental action"), they draw the reader into the world of standards quickly and keep that momentum throughout the book. And they give examples to crystallize reader's understanding. Hence, "primer" in the title is well justified.

While the book keeps overall engineering standards in view (and thus not excluding information technology, software, building codes, etc.), it does lean towards mechanical engineering standards when it comes to details. It is understandable because the book is published by ASME.

The book is neatly organized to make the reader understand the whole spectrum of engineering standards. The second chapter discusses General Consensus Standards and Codes. These are important for industry practitioners because professional societies accredited by American National Standards Institute (ANSI) develop these standards. ASME and IEEE are two such societies accredited by ANSI. The third chapter introduces Limited Consensus Standards, which are for use internally by specific organizations. Government organizations such as National Aeronautics and Space Administration (NASA) or private industries have such standards. These standards can be proprietary or non-proprietary. As opposed to these two categories of standards, Jurisdictional Standards are to be followed by all organizations as they have legal implications. An example is standards imposed by Occupational Safety and Health Administration (OSHA). These are discussed in Chapter 5. Chapter 6 contains detailed description of types of standards such as prescriptive, performance, etc. Chapters 7 contains practically useful information about how to interpret standards and how to get relief from standards when it is necessary. The last chapter describes the characteristics of a good standard. It is the key chapter for those who want to develop new standards. The book also has an index, glossary, and a list of acronyms. It also features cartoons in a few chapters to make a point with visual appeal.

The expanded textbook edition of this book, published by Wiley in 2018, has three new chapters and four appendices. The new chapters describe the standard development process, conformity assessment, and how to get involved in the standards development process. It is therefore particularly useful for anyone who want to develop new standards. Appendices also contain pertinent information such as the list of organizations that issue limited consensus standards, jurisdictional standard agencies, etc.

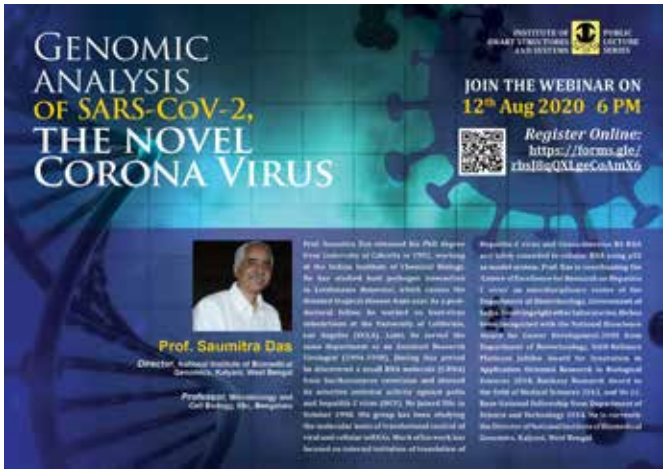
Overall, this is a good book that gives a comprehensive information about engineering standards.

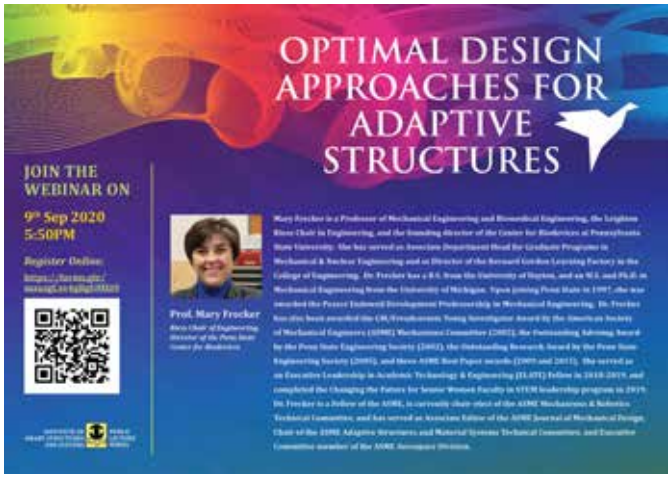
8 ISSS Webinar

With the entire scientific community battling through COVID-19, students away from their research work there was a serious concern to each and every individual to find a way out of this and look for alternatives for progress in their respective work space. The Institute of Smart Structures and Systems have come up with an idea of bringing all the scientific community on one platform in the form of conducting webinars online by sharing and transferring knowledge named as SUKSHMA WEBINARS. SUKSHMA means “Small and Subtle”.

Various topics such as Gas sensors, Genomic analysis of SARS-COV-2, Biophysics of proteins, Adaptive structures, Sensors and Computing, Robotics, Artificial Intelligence, Renewable Energy, Building an Artificial Brian, Molecular level Interaction, Deposition of Functional materials and Neural electronics have been delivered by eminent speakers across the globe. The webinars are conducted on 2nd and 4th Wednesday of the month.

With the consent of the speaker, webinars were recorded and has been uploaded in our YouTube channel
https://www.youtube.com/channel/UC7yimgRQEaZPvLgqqG2LJvQ
As part of a webinar series, a panel discussion on “Early Education on (K-12) in INDIA has been conducted.”





What is New in ISSS?

Recently ISSS has signed an MoU agreement with IEEE. Through this initiative IEEE Sensors Council in India and ISSSS have decided to jointly conduct international conferences on Sensors and Sensor Systems. The IEEE Sensors council in association with ISSS is organising the APSCON-23 conference on Applied Sensing during January 2023 in Bangalore.

Join us for the inaugural Applied Sensing Conference (APSCON) on January 23- 25, 2023 in Bengaluru, INDIA.

APSCON will be a three-day event with one day of industry engagement and two days of technical sessions. The IEEE Conference has ISSS as the Technical Co-sponsor.

Contemporary National News on Technology

Recently the Government of India has shared an exciting announcement mentioning that Vedanta charts $8 billion chip manufacturing plan via Foxconn JV [1,2,3]. This announcement is expected to give a significant boost to chip manufacturing opportunities in India. We have included an article on this topic in our present issue of Sukshma. We wish to bring more insightful articles on that matter in our coming issues of Sukshma.

https://economictimes.indiatimes.com/industry/cons-products/electronics/vedanta-charts-8-billion-chip-manufacturing-plan-via-foxconn-jv/articleshow/89672585.cms

https://www.livemint.com/industry/manufacturing/vedanta-and-foxconn-to-form-jv-to-manufacture-semiconductors-11644848510887.html

https://theprint.in/opinion/vedantas-latest-chip-venture-with-foxconn-is-just-a-little-more-than-a-piece-of-paper/833460/

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